Analog Devices

2

Overview

This chapter describes the analog devices supported by PSpice A/D and PSpice. The following information is provided:

- device type
- format
- usage
- library location

Analog Devices

This chapter describes the different types of analog devices supported by PSpice and PSpice A/D. These device types include analog primitives, independent and controlled sources, and subcircuit calls. Each device type is described separately, and each description includes the following information as applicable:

- A description, and example of, the proper netlist syntax.
- The corresponding model types and their description.
- The corresponding list of model parameters and their descriptions.
- The equivalent circuit diagram and characteristic equations for the model (as required).
- References to publications on which the model is based.

These analog devices include all of the standard circuit components that normally are not considered part of the two-state (binary) devices that are found in the digital devices.

The model library consists of analog models of off-the-shelf parts that can be used directly in circuits that are being developed. Refer to the Library Reference Manual for device models and in which library they can be found. The model library includes models implemented using the .MODEL statement and macromodels implemented as subcircuits with the .SUBCKT statement.

This chapter includes a summary table, Table 2-1, which lists all of the analog device primitives supported by the simulator. Each primitive is described in detail in the sections following the table.

Device Types

PSpice supports many types of analog devices, including sources and general subcircuits. PSpice A/D also supports digital devices. The supported devices are categorized into device types. each of which can have one or more model types. For example, the BJT device type has three model types: NPN, PNP, and LPNP (Lateral PNP). The description of each devices type includes a description of any of the model types it supports.

The device declarations in the netlist always begin with the name of the individual device (instance). The first letter of the name determines the device type. What follows the name depends on the device type and its requested characteristics. Table 2-1 summarizes the device types and the general form of their declaration formats.

Note *The "Device Type" column in the table includes the designator (letter) used in the device modeling.*

Table 2-1 *Analog Device Summary*

Device Type	Letter	Declaration Format	Page
Bipolar Transistor	Q	Q*<name> <collector node> <base node> <emitter node> + [substrate node] <model name> [area value]*	2-54
Capacitor	C	C*<name> <+ node> <- node> [model name] <value>* + [IC=*<initial value>*]	2-13
Voltage-Controlled Voltage Source	E	E*<name> <+ node> <- node> <+ controlling node> + <- controlling node> <gain>* (additional Analog Behavioral Modeling forms: VALUE, TABLE, LAPLACE, and FREQ; additional POLY form)	2-18
Voltage-Controlled Current Source	G	G*<name> <+ node> <- node> <+ controlling node> + <- controlling node> <transconductance>* (additional Analog Behavioral Modeling forms: VALUE, TABLE, LAPLACE, and FREQ; additional POLY form)	2-18
Current-Controlled Current Source	F	F*<name> <+ node> <- node> <controlling V device name> + <gain>* (additional POLY form)	2-20
Current-Controlled Switch	W	W*<name> <+ switch node> <- switch node> + <controlling V device name> <model name>*	2-67

Table 2-1 *Analog Device Summary (continued)*

Device Type	Letter	Declaration Format	Page
Current-Controlled Voltage Source	H	H*<name> <+ node> <- node> <controlling V device name> + <transresistance>* (additional POLY form)	2-20
Digital Input	N	N*<name> <interface node> <low level node> <high level node> + <model name> <input specification>*	2-47
Digital Output	O	O*<name> <interface node> <low level node> <high level node> + <model name> <output specification>*	2-50
Digital Primitive*	U	U*<name> <primitive type> ([parameter value]*) + <digital power node> <digital ground node> <node>* + <timing model name>*	2-66
Diode	D	D*<name> <anode node> <cathode node> <model name>* [area value]	2-15
GaAsFET	B	B*<name> <drain node> <gate node> <source node> + <model name>* [area value]	2-6
Independent Current Source & Stimulus	I	I*<name> <+ node> <- node> [[DC] <value>] + [AC <magnitude value>* [phase value]] [transient specification]	2-21
Independent Voltage Source & Stimulus	V	V*<name> <+ node> <- node> [[DC] <value>] + [AC <magnitude value>* [phase value]] [transient specification]	2-21
Inductor	L	L*<name> <+ node> <- node> [model name] <value> +* [IC=*<initial value>]*	2-35
Inductor Coupling	K	K*<name>* L*<inductor name>* <L*<inductor name>>** + *<coupling value>* K*<name>* <L*<inductor name>>** *<coupling value>* + *<model name>* [size value]	2-31
JFET	J	J*<name> <drain node> <gate node> <source node> + <model name>* [area value]	2-26

Table 2-1 *Analog Device Summary (continued)*

Device Type	Letter	Declaration Format	Page
MOSFET	M	M*<name> <drain node> <gate node> <source node> + <bulk/substrate node> <model name>* + [common model parameter]*	2-36
Resistor	R	R*<name> <+ node> <- node>* [model name] *<value>*	2-61
Subcircuit Call	X	X*<name>* [node]* *<subcircuit name>*	2-70
Transmission Line	T	T*<name> <A port + node> <A port - node> + <B port + node> <B port - node>*	2-64
Transmission Line Coupling	K	K*<name>* T*<line name>* <T*<line name>>** + CM=*<coupling capacitance>* LM=*<coupling inductance>*	2-31
Voltage-Controlled Switch	S	S*<name> <+ switch node> <- switch node> + <+ controlling node> <- controlling node> <model name>*	2-62

*The Digital Primitive and Digital Stimulus device types are generic in form. They have flexible syntax, and can refer to numerous different devices.

GaAsFET

General Form

B*<name> <drain node> <gate node> <source node>*
+ <model name> [*area value*]

Examples

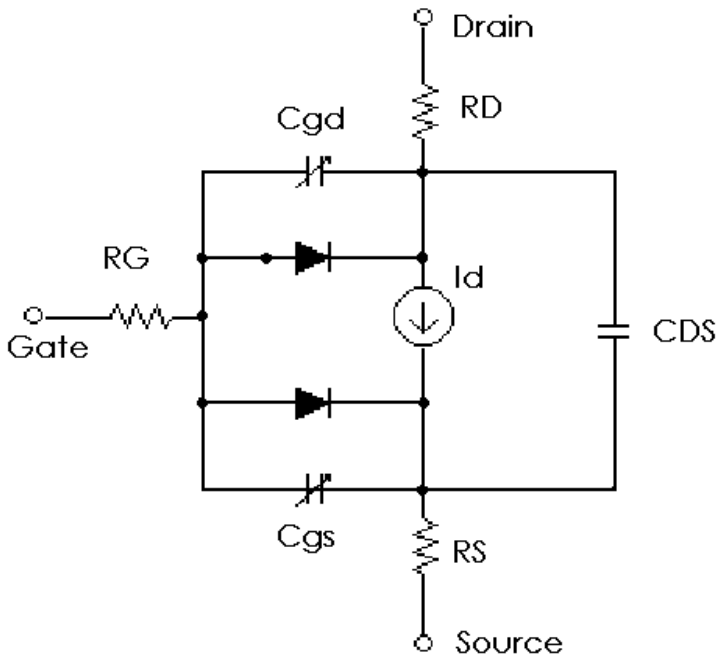
BIN 100 10 0 GFAST
B13 22 14 23 GNOM 2.0

Model Form

.MODEL <model name> GASFET [model parameters]

As shown in Figure 2-1, the GaAsFET is modeled as an intrinsic FET using an ohmic resistance (**RD**/area) in series with the drain, another ohmic resistance (**RS**/area) in series with the source, and another ohmic resistance (**RG**) in series with the gate. The [area value] is the relative device area and defaults to 1.

Figure 2-1 *GaAsFET Mode*



The **LEVEL** model parameter selects between different models for the intrinsic GaAsFET:

GaAsFET LEVELS	Definition
LEVEL=1	"Curtice" model (see reference [1]).
LEVEL=2	"Raytheon" or "Statz" model (see reference [3]) and is equivalent to the GaAsFET model in SPICE3.

Model Parameters

Table 2-2 *GaAsFET Model Parameters for All Levels*

Model Parameters	Description	Units	Default
LEVEL	Model index (1 or 2)		1
VTO	Pinchoff voltage	volt $^{-2}$	.5
ALPHA	Saturation voltage parameter	volt $^{-1}$	2.0
BETA	Transconductance coefficient	amp/volt ^{2}	0.1
B	Doping tail extending parameter (LEVEL=2 *only*)	volt $^{-1}$	0.3
LAMBDA	Channel-length modulation	volt $^{-1}$	0
TAU	Conduction current delay time	sec	0
RG	Gate ohmic resistance	ohm	0
RD	Drain ohmic resistance	ohm	0
RS	Source ohmic resistance	ohm	0
IS	Gate *p-n* saturation current	amp	1E-14
N	Gate *p-n* emission coefficient		1
M	Gate *p-n* grading coefficient		0.5
VBI	Gate *p-n* potential	volt	1.0
CGD	Zero-bias gate-drain *p-n* capacitance	farad	0
CGS	Zero-bias gate-source *p-n* capacitance	farad	0
CDS	Drain-source capacitance	farad	0
FC	Forward-bias depletion capacitance coefficient		0.5
VTOTC	VTO temperature coefficient	volt/°C	0
BETATCE	BETA exponential temperature coefficient	%/°C	0
KF	Flicker noise coefficient		0
AF	Flicker noise exponent		1

Equations

In the following equations:

Vgs = intrinsic gate-intrinsic source voltage
Vgd = intrinsic gate-intrinsic drain voltage
Vds = intrinsic drain-intrinsic source voltage
Vt = k·T/q (thermal voltage)
k = Boltzmann constant
q = electron charge
T = analysis temperature (°K)
Tnom = nominal temperature (set using .OPTIONS TNOM=)

These equations describe an N-channel GaAsFET.
Positive current is current flowing into a terminal (for example, positive drain current flows from the drain through the channel to the source).

DC Currents

Ig = gate current = *area*·(Igs+Igd)
Igs = gate-source leakage current
Igd = gate-drain leakage current
Igs = **IS**·(e $^{Vgs/(\mathbf{N}\cdot Vt)}$ -1)
Igd = **IS**·(e $^{Vgd/(\mathbf{N}\cdot Vt}$) -1)

Equations for Idrain: LEVEL=1

For: Vds ≥ 0 (normal mode)
and: Vgs - **VTO** < 0 (cutoff region)
Idrain = 0
and: Vgs - **VTO** ≥ 0 (linear & saturation region)
Idrain = **BETA**·(1+**LAMBDA**·Vds)·(Vgs-**VTO**)^2 ·tanh(**ALPHA**·Vds)
For: Vds < 0 (inverted mode)
Switch the source and drain in equations (above).

Equations for Idrain: LEVEL=2

For: Vds ≥ 0 (normal mode)
and: Vgs - **VTO** < 0 (cutoff region)
Idrain = 0
and: Vgs - **VTO** ≥ 0 (linear & saturation region)
Idrain = **BETA**·(1+**LAMBDA**·Vds)·(Vgs-**VTO**)^2 ·Kt/(1+**B**·(Vgs-**VTO**))
where Kt (a polynomial approximation of tanh) is:
for: 0 < Vds < 3/**ALPHA** (linear region)
Kt = 1 - (1 - Vds·**ALPHA**/3)^3
for: Vds ≥ 3/**ALPHA** (saturation region)
Kt = 1
For: Vds < 0 (inverted mode)
Switch the source and drain in equations (above).

Capacitance[1]

Cds = drain-source capacitance = *area*·**CDS**

Equations for Cgs and Cgd: LEVEL=1

Cgs = gate-source capacitance

For: Vgs ≤ **FC**·**VBI**

$Cgs = area \cdot CGS \cdot (1 - Vgs/VBI)^{-M}$

For: Vgs > **FC**·**VBI**

$Cgs = area \cdot CGS \cdot (1-FC)^{-(1+M)} \cdot (1 - FC \cdot (1+M) + M \cdot Vgs/VBI)$

Cgd = gate-drain capacitance

For: Vgd ≤ **FC**·**VBI**

$Cgd = area \cdot CGD \cdot (1 - Vgd/VBI)^{-M}$

For: Vgd > **FC**·**VBI**

$Cgd = area \cdot CGD \cdot (1-FC)^{-(1+M)} \cdot (1 - FC \cdot (1+M) + M \cdot Vgd/VBI)$

Equations for Cgs and Cgd: LEVEL=2

Cgs = gate-source capacitance = $area \cdot (CGS \cdot K2 \cdot K1/(1 - Vn/VBI)^{1/2} + CGD \cdot K3)$

Cgd = gate-drain capacitance = $area \cdot (CGS \cdot K3 \cdot K1/(1 - Vn/VBI)^{1/2} + CGD \cdot K2)$

where

$K1 = (1 + (Ve - VTO)/((Ve - VTO)^2 + VDELTA^2)^{1/2})/2$

$K2 = (1 + (Vgs - Vgd)/((Vgs - Vgd)^2 + (1/ALPHA)^2)^{1/2})/2$

$K3 = (1 - (Vgs - Vgd)/((Vgs - Vgd)^2 + (1/ALPHA)^2)^{1/2})/2$

$Ve = (Vgs + Vgd + ((Vgs - Vgd)^2 + (1/ALPHA)^2)^{1/2})/2$

If: $(Ve + VTO + ((Ve - VTO)^2 + VDELTA^2)^{1/2})/2 < VMAX$

$Vn = (Ve + VTO + ((Ve - VTO)^2 + VDELTA^2)^{1/2})/2$

else: $Vn = VMAX$

1. All capacitances are between terminals of the intrinsic GaAsFET (that is, to the inside of the ohmic drain, source, and gate resistances).

Temperature Effects

For all levels:

$$\mathbf{VTO}(T) = \mathbf{VTO} + \mathbf{VTOTC} \cdot (T - Tnom)$$

$$\mathbf{BETA}(T) = \mathbf{BETA} \cdot 1.01^{\mathbf{BETATCE} \cdot (T - Tnom)}$$

$$\mathbf{IS}(T) = \mathbf{IS} \cdot e^{(T/Tnom - 1) \cdot \mathbf{EG}/(\mathbf{N} \cdot Vt)} \cdot (T/Tnom)^{\mathbf{XTI}/\mathbf{N}}$$

$$\mathbf{VBI}(T) = \mathbf{VBI} \cdot T/Tnom - 3 \cdot Vt \cdot ln(T/Tnom) - \mathbf{EG}(Tnom) \cdot T/Tnom + \mathbf{EG}(T)$$

where $\mathbf{EG}(T)$ = silicon bandgap energy = $1.16 - .000702 \cdot T^2/(T+1108)$

$$\mathbf{CGS}(T) = \mathbf{CGS} \cdot (1 + \mathbf{M} \cdot (.0004 \cdot (T - Tnom) + (1 - \mathbf{VBI}(T)/\mathbf{VBI})))$$

$$\mathbf{CGD}(T) = \mathbf{CGD} \cdot (1 + \mathbf{M} \cdot (.0004 \cdot (T - Tnom) + (1 - \mathbf{VBI}(T)/\mathbf{VBI})))$$

Noise

Noise is calculated assuming a one hertz bandwidth, using the following spectral power densities (per unit bandwidth):

the parasitic resistances, **RS**, **RD**, and **RG** generate thermal noise ...

$$Is^2 = 4 \cdot k \cdot T/(\mathbf{RS}/area)$$

$$Id^2 = 4 \cdot k \cdot T/(\mathbf{RD}/area)$$

$$Ig^2 = 4 \cdot k \cdot T/\mathbf{RG}$$

the intrinsic GaAsFET generates shot and flicker noise ...

$$Id^2 = 4 \cdot k \cdot T \cdot gm \cdot 2/3 + \mathbf{KF} \cdot Id^{\mathbf{AF}}/FREQUENCY$$

where $gm = dIdrain/dVgs$ (at the DC bias point)

References

For more information on this GaAsFET model, refer to:

[1] W. R. Curtice, “A MESFET model for use in the design of GaAs integrated circuits,” *IEEE Transactions on Microwave Theory and Techniques*, MTT-28, 448-456 (1980).

[2] S. E. Sussman-Fort, S. Narasimhan, and K. Mayaram, “A complete GaAs MESFET computer model for SPICE,” *IEEE Transactions on Microwave Theory and Techniques*, MTT-32, 471-473 (1984).

[3] H. Statz, P. Newman, I. W. Smith, R. A. Pucel, and H. A. Haus, “GaAs FET Device and Circuit Simulation in SPICE,” *IEEE Transactions on Electron Devices*, ED-34, 160-169 (1987).

[4] A. J. McCamant, G. D. McCormack, and D. H. Smith, “An Improved GaAs MESFET Model for SPICE,” *IEEE Transactions on Microwave Theory and Techniques*, June 1990 (est).

[5] A. E. Parker and D. J. Skellern “Improved MESFET Characterization for Analog Circuit Design and Analysis,” 1992 *IEEE GaAs IC Symposium Technical Digest*, pp. 225-228, Miami Beach, October 4-7, 1992.

[6] A. E. Parker, “Device Characterization and Circuit Design for High Performance Microwave Applications,” *IEE EEDMO’93*, London, October 18, 1993.

[7] D. H. Smith, “An Improved Model for GaAs MESFETs,” Publication forthcoming. (Copies available from TriQuint Semiconductors Corporation or MicroSim.)

Capacitor

General Form C*<name> <(+) node> <(-) node> [model name] <value>*
+ [IC=*<initial value>*]

Examples
CLOAD 15 0 20pF
C2 1 2 .2E-12 IC=1.5V
CFDBCK 3 33 CMOD 10pF

Model Form .MODEL *<model name>* CAP [*model parameters*]

Table 2-3 Capacitor Model Parameters

Model Parameters*	Description	Units	Default
C	Capacitance multiplier		1
VC1	Linear voltage coefficient	volt $^{-1}$	0
VC2	Quadratic voltage coefficient	volt $^{-2}$	0
TC1	Linear temperature coefficient	°C $^{-1}$	0
TC2	Quadratic temperature coefficient	°C $^{-2}$	0

(+) and (-) nodes Define the polarity when the capacitor has a positive voltage across it. The first node listed (or pin one in Schematics), is defined as positive. The voltage across the component is therefore defined as the first node voltage less the second node voltage.
Positive current flows from the (+) node through the capacitor to the (-) node. Current flow from the first node through the component to the second node is considered positive

[model name] If *[model name]* is left out then <*value*> is the capacitance in farads. If [*model name*] is specified, then the capacitance is given by the formula

<*value*>·C·(1+**VC1**·V+**VC2**·V 2)·(1+**TC1**·(T-Tnom)+**TC2**·(T-Tnom)2)

where <*value*> is normally positive (though it can be negative, but *not zero*). “Tnom” is the nominal temperature (set using TNOM option).

<*initial value*> The initial voltage across the capacitor during the bias point calculation. It can also be specified in a circuit file using a .IC command as follows:

.IC V(+*node, -node*) <*initial value*>

For details on using the .IC command in a circuit file, see page 1-12 of this manual, and refer to your PSpice user’s guide, for more information.

Noise

The capacitor does not have a noise model.

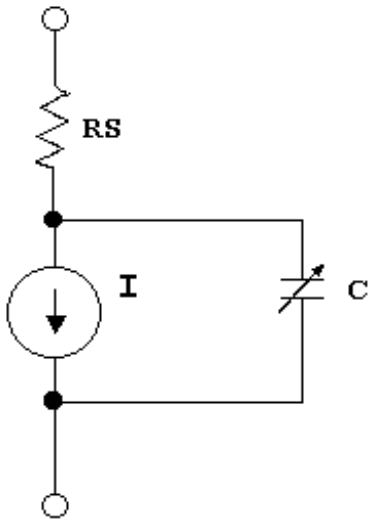
Diode

General Form D<*name*> <*(+) node*> <*(-) node*> <*model name*> [*area value*]

Examples
DCLAMP 14 0
DMOD D13 15 17 SWITCH 1.5

Model Form .MODEL < *model name*> D [*model parameters*]

Figure 2-2 *Diode Model*



As shown, the diode is modeled as an ohmic resistance (RS/area) in series with an intrinsic diode. The <*(+) node*> is the anode and <*(-) node*> is the cathode. Positive current is current flowing from the anode through the diode to the cathode. The [area value] scales IS, **ISR, IKF,RS, CJO**, and **IBV**, and defaults to 1. **IBV** and **BV** are both specified as positive values.

Model Parameters

Table 2-4 *Diode Model Parameters*

Model Parameters*	Description	Unit	Default
IS	Saturation current	amp	1E-14
N	Emission coefficient		1
ISR	Recombination current parameter	amp	0
NR	Emission coefficient for ISR		2
IKF	High-injection “knee” current	amp	infinite
BV	Reverse breakdown “knee” voltage	volt	infinite
IBV	Reverse breakdown “knee” current	amp	1E-10
RS	Parasitic resistance	ohm	0
TT	Transit time	sec	0
CJO	Zero-bias *p-n* capacitance	farad	0
VJ	*p-n* potential	volt	1
M	*p-n* grading coefficient		0.5
FC	Forward-bias depletion capacitance coefficient		0.5
EG	Bandgap voltage (barrier height)	eV	1.11
XTI	IS temperature exponent		3
TIKF	IKF temperature coefficient (linear)	$°C^{-1}$	0
TRS1	RS temperature coefficient (linear)	$°C^{-1}$	0
TRS2	RS temperature coefficient (quadratic)	$°C^{-2}$	0
KF	Flicker noise coefficient		0
AF	Flicker noise exponent		1

Equations

In the following equations:

Vd = voltage across the intrinsic diode only
Vt = k·T/q (thermal voltage)
k = Boltzmann's constant
q = electron charge
T = analysis temperature (°K)
Tnom = nominal temperature (set using TNOM option)

Other variables are from the model parameter list.

DC Current

Id = *area*·(Ifwd - Irev)

Ifwd = forward current = Inrm·Kinj + Irec·Kgen

Inrm = normal current = $IS\cdot(e^{Vd/(N\cdot Vt)} -1)$

Kinj = high-injection factor

For: **IKF** > 0

$Kinj = (\mathbf{IKF}/(\mathbf{IKF}+Inrm))^{1/2}$

otherwise

Kinj = 1

Irec = recombination current = $\mathbf{ISR}\cdot(e^{Vd/(NR\cdot Vt)} -1)$

Kgen = generation factor = $((1-Vd/VJ)^2 +0.005)^{M/2}$

Irev = reverse current = $Irev_{high} + Irev_{low}$

$Irev_{high} = \mathbf{IBV}\cdot e^{-(Vd+BV)/(NBV\cdot Vt)}$

$Irev_{low} = \mathbf{IBVL}\cdot e^{-(Vd+BV)/(NBVL\cdot Vt)}$

Capacitance

Cd = Ct + *area*·Cj

Ct = transit time capacitance = **TT**·Gd

where Gd = DC conductance

Cj = junction capacitance

For: $Vd \le \mathbf{FC}\cdot\mathbf{VJ}$

$Cj = \mathbf{CJO}\cdot(1-Vd/VJ)^{-M}$

For: $Vd > FC\cdot VJ$

$Cj = \mathbf{CJO}\cdot(1-\mathbf{FC})^{-(1+M)}\cdot(1-\mathbf{FC}\cdot(1+\mathbf{M})+\mathbf{M}\cdot Vd/\mathbf{VJ})$

Voltage-Controlled Voltage Source and Voltage-Controlled Current Source

Note

The Voltage-Controlled Voltage Source (E) and the Voltage-Controlled Current Source (G) devices have the same syntax. For a Voltage-Controlled Current Source just substitute a "G" for the "E". The "G" device generates a current, whereas, the "E" device generates a voltage.

General Form

E*<name> <(+) node> <(-) node> <(+) controlling node> <(-) controlling node> <gain>*

E*<name> <(+) node> <(-) node>* POLY(*<value>*)
*+ < <(+) controlling node> <(-) controlling node> >**
*+ < <polynomial coefficient value> >**

E*<name> <(+) <node> <(-) node>* VALUE *= { <expression> }*

E*<name> <(+) <node> <(-) node>* TABLE *{ <expression> } =*
*+ < <input value>,<output value> >**

E*<name> <(+) node> <(-) node>* LAPLACE *{ <expression> } =*
+ { <transform> }

E*<name> <(+) node> <(-) node>* FREQ *{ <expression> } =*
*[*KEYWORD*] + < <frequency value>,<magnitude value>,<phase value> >* + [*DELAY *= <delay value>]*

Examples

```
EBUFF   1   2   10   11   1.0
EAMP   13   0   POLY(1)   26   0   0   500
ENONLIN   100   101   POLY(2)   3   0   4   0   0.0   13.6   0.2   0.005
```

The first form and the first two examples apply to the linear case. The second form and the last example are for the nonlinear case.

POLY(<*value*>) Specifies the number of dimensions of the polynomial. The number of pairs of controlling nodes must be equal to the number of dimensions.

(+) and (-) nodes Output nodes. Positive current flows from the (+) node through the source to the (-) node.

The <*(+) controlling node*> and <*(-) controlling node*> are in pairs and define a set of controlling voltages. A particular node can appear more than once, and the output and controlling nodes need not be different. The TABLE form has a maximum size of 2048 input/output value pairs.

For the linear case, there are two controlling nodes and these are followed by the gain. For all cases, including the nonlinear case (POLY), refer to your PSpice user's guide.

Expressions **cannot** be used for linear and polynomial coefficient values in a voltage-controlled voltage source device statement.

Current-Controlled Current Source and Current-Controlled Voltage Source

Note *The Current-Controlled Current Source (F) and the Current-Controlled Voltage Source (H) devices have the same syntax. For a Current-Controlled Voltage Source just substitute a "H" for the "F". The "H" device generates a voltage, whereas, the "F" device generates a current.*

General Form

F*<name> <(+) node> <(-) node>*
+ <controlling V device name> <gain>

F*<name> <(+) node> <(-) node>* POLY*(<value>)*
*+ <controlling V device name>**
*+ < <polynomial coefficient value> >**

(+) and (-) These nodes are the output nodes. A positive current flows from the (+) node through the source to the (-) node. The current through the controlling voltage source determines the output current. The controlling source must be an independent voltage source (V device), although it need not have a zero DC value.

For the linear case, there must be one controlling voltage source and its name is followed by the gain. For all cases, including the nonlinear case (POLY), refer to your PSpice user's guide.

Note *Expressions cannot be used for linear and polynomial coefficient values in a current-controlled current source device statement.*

Examples

```
FSENSE   1   2   VSENSE   10.0
FAMP   13   0   POLY(1)   VIN   0   500
FNONLIN   100   101   POLY(2)   VCNTRL1   VCINTRL2   0.0   13.6   0.2   0.005
```

The first form and the first two Examples apply to the linear case.

The second form and the last example are for the nonlinear case.

POLY(<value>) specifies the number of dimensions of the polynomial.

The number of controlling voltage sources must be equal to the number of dimensions.

Independent Current Source & Stimulus and Independent Voltage Source & Stimulus

Note *The Independent Current Source & Stimulus (I) and the Independent Voltage Source & Stimulus (V) devices have the same syntax. For an Independent Voltage Source & Stimulus just substitute a "V" for the "I". The "V" device functions identically and has the same syntax as the "I" device, except that it generates voltage instead of current.*

General Form

I*<name> <(+) node> <(-) node>*
+ [[DC] *<value>]*
+ [AC *<magnitude value> [phase value]]*
+ [transient specification]

Examples

```
IBIAS     13     0     2.3mA
IAC        2     3     AC   .001
IACPHS     2     3     AC   .001   90
IPULSE     1     0     PULSE(-1mA   1mA   2ns   2ns   2ns   50ns   100ns)
I3        26    77     DC   .002   AC   1   SIN(  .002   .002   1.5MEG)
```

This element is a current source. Positive current flows from the (+) node through the source to the (-) node: in the first example, IBIAS drives node 13 to have a *negative* voltage. The default value is zero for the DC, AC, and transient values. None, any, or all of the DC, AC, and transient values can be specified. The AC phase value is in degrees. The pulse and exponential examples are explained later in this section.

[*transient specification*] If present, they must be one of:

EXP (<*parameters*>) for an exponential waveform

PULSE (<*parameters*>) for a pulse waveform

PWL (<*parameters*>) for a piecewise linear waveform

SFFM (<*parameters*>) for a frequency-modulated waveform

SIN (<*parameters*>) for a sinusoidal waveform

The variables TSTEP and TSTOP, which are used in defaulting some waveform parameters, are set by the .TRAN command. TSTEP is <*print step value*> and TSTOP is <*final time value*>. The .TRAN command can be anywhere in the circuit file; it need not come after the voltage source.

Independent Current Source & Stimulus (EXP)

General Form EXP (<i1> <i2> <td1> <tc1> <td2> <tc2>)

Example

```
IRAMP   10   5   EXP(1   5   1   .2   2   .5)
```

Table 2-5 *Independent Current Source and Stimulus Exponential Waveform Parameters*

Parameters	Description	Units	Default
<i1>	Initial current	amp	none
<i2>	Peak current	amp	none
<td1>	Rise (fall) delay	sec	0
<tc1>	Rise (fall) time constant	sec	**TSTEP**
<td2>	Fall (rise) delay	sec	<td1>+**TSTEP**
<tc2>	Fall (rise) time constant	sec	**TSTEP**

The EXP form causes the current to be <i1> for the first <td1> seconds. Then, the current decays exponentially from <i1> to <i2> using a time constant of <tc1>. The decay lasts td2-td1 seconds. Then, the current decays from <i2> back to <i1> using a time constant of <tc2>.

Independent Current Source & Stimulus (PULSE)

General Form PULSE (<i1> <i2> <td> <tr> <tf> <pw> <per>)

Examples

```
ISW   10   5   PULSE(1A   5A   1sec   .1sec   .4sec   .5sec   2sec)
```

Table 2-6 *Independent Current Source and Stimulus Pulse Waveform Parameters*

Parameters	Description	Units	Default
<i1>	Initial current	amp	none
<i2>	Pulsed current	amp	none
<per>	Period	sec	**TSTOP**
<pw>	Pulse width	sec	**TSTOP**
<td>	Delay	sec	0
<tf>	Fall time	sec	**TSTEP**
<tr>	Rise time	sec	**TSTEP**

The PULSE form causes the current to start at <i1>, and stay there for <td> seconds. Then, the current goes linearly from <i1> to <i2> during the next <tr> seconds, and then the current stays at <i2> for <pw> seconds. Then, it goes linearly from <i2> back to <i1> during the next <tf> seconds. It stays at <i1> for per-(tr+pw+tf) seconds, and then the cycle is repeated except for the initial delay of <td> seconds.

Independent Current Source & Stimulus (PWL)

General Form PWL (*corner_points*)

where *corner_points* are: (<tn>, <in>)

Examples

```
I1  1  2  PWL (0   1   1.2   5   1.4   2   2   4   3   1)
```

Table 2-7 *Independent Voltage Source and Stimulus PWL Waveform Parameters*

Parameters*	Description	Units	Default
<tn>	Time at corner	seconds	None
<vn>	Voltage at corner	volts	None

The PWL form describes a piecewise linear waveform. Each pair of time-current values specifies a corner of the waveform. The current at times between corners is the linear interpolation of the currents at the corners.

Independent Current Source & Stimulus (SFFM)

General Form SFFM (<ioff> <iampl> <fc> <mod> <fm>)

Examples IMOD 10 5 SFFM(2 1 8Hz 4 1Hz)

Table 2-8 *Independent Current Source and Stimulus Frequency-Modulated Waveform Parameters*

Parameter	Description	Units	Default
<ioff>	Offset current	amp	none
<iampl>	Peak amplitude of current	amp	none
<fc>	Carrier frequency	hertz	1/**TSTOP**
<mod>	Modulation index		0
<fm>	Modulation frequency	hertz	1/**TSTOP**

The SFFM (Single-Frequency FM) form causes the current, to follow this formula

$$ioff + iampl \cdot sin(2\pi \cdot fc \cdot TIME + mod \cdot sin(2\pi \cdot fm \cdot TIME))$$

Independent Current Source & Stimulus (SIN)

General Form SIN (<ioff> <iampl> <freq> <td> <df> <phase>)

Examples ISIG 10 5 SIN(2 2 5Hz 1sec 1 30)

Table 2-9 *Independent Current Source and Stimulus Sinusoidal Waveform Parameters*

Parameters	Description	Units	Default
<ioff>	Offset current	amp	none
<iampl>	Peak amplitude of current	amp	none
<freq>	Frequency	hertz	1/**TSTOP**
<td>	Delay	sec	0
<df>	Damping factor	sec^{-1}	0
<phase>	Phase	degree	0

The sinusoidal (SIN) waveform causes the current to start at <ioff> and stay there for <td> seconds.
Then, the current becomes an exponentially damped sine wave. The waveform could be described by the following formulas.

$$ioff+iampl\cdot sin(2\pi\cdot(freq\cdot(TIME-td)+phase/360°))\cdot e^{-(TIME-td)\cdot df}$$

Note *The SIN waveform is for transient analysis only. It does not have any effect during AC analysis. To give a value to a current during AC analysis, use an AC specification, such as*

```
IAC   3   0   AC   1mA
```

where IAC has an amplitude of one milliampere during AC analysis, and can be zero during transient analysis. For transient analysis use (for example)

```
ITRAN 3 0 SIN(0 1mA 1kHz)
```

where ITRAN has an amplitude of one milliampere during transient analysis and is zero during AC analysis. Refer to your PSpice user's guide.

Junction FET

General Form

J*<name> <drain node> <gate node> <source node>*
+ <model name> [area value]

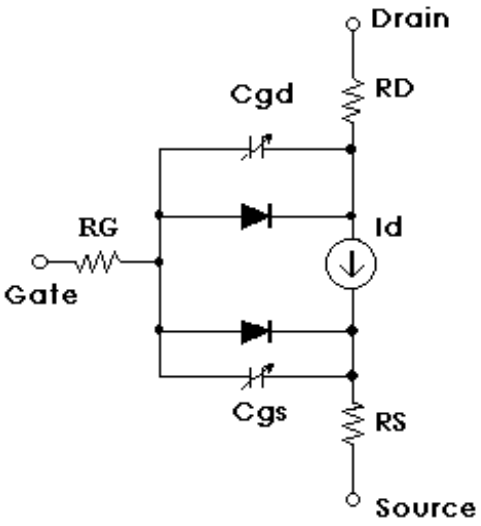
Examples

```
JIN   100   1   0   JFAST
J13   22   14   23   JNOM   2.0
```

Model Form

.MODEL *<model name>* NJF *[model parameters]*
.MODEL *<model name>* PJF *[model parameters]*

Figure 2-3 *JFET Model*



As shown in Figure 2-3, the JFET is modeled as an intrinsic FET using an ohmic resistance (**RD**/*area*) in series with the drain, and using another ohmic resistance (**RS**/*area*) in series with the source. Positive current is current flowing into a terminal. The [*area value*] is the relative device area and defaults to 1.

Table 2-10 *Junction FET Model Parameters*

Model Parameters	Description	Units	Default
AF	Flicker noise exponent		1
ALPHA	Ionization coefficient	volt $^{-1}$	0
BETA	Transconductance coefficient	amp/volt ^{2}	1E-4
BETATCE	BETA exponential temperature coefficient	%/°C	0
CGD	Zero-bias gate-drain *p-n* capacitance	farad	0
CGS	Zero-bias gate-source *p-n* capacitance	farad	0
FC	Forward-bias depletion capacitance coefficient		0.5
IS	Gate *p-n* saturation current	amp	1E-14
ISR	Gate *p-n* recombination current parameter	amp	0
KF	Flicker noise coefficient		0
LAMBDA	Channel-length modulation	volt $^{-1}$	0
M	Gate *p-n* grading coefficient		0.5
N	Gate *p-n* emission coefficient		1
NR	Emission coefficient for ISR		2
PB	Gate *p-n* potential	volt	1.0
RD	Drain ohmic resistance	ohm	0
RS	Source ohmic resistance	ohm	0
VK	Ionization “knee” voltage	volt	0
VTO	Threshold voltage	volt	-2.0
VTOTC	VTO temperature coefficient	volt/°C	0
XTI	IS temperature coefficient		3

Note ***VTO < 0 means the device is a depletion-mode JFET (for both N-channel and P-channel) and VTO > 0 means the device is an enhancement-mode JFET. This conforms to U.C. Berkeley SPICE.***

Equations

In the following equations:

Vgs = intrinsic gate-intrinsic source voltage
Vgd = intrinsic gate-intrinsic drain voltage
Vds = intrinsic drain-intrinsic source voltage
Vt = $k \cdot T/q$ (thermal voltage)
k = Boltzmann's constant
q = electron charge
T = analysis temperature (°K)
Tnom = nominal temperature (set using TNOM option)

Other variables are from the model parameter list. These equations describe an N-channel JFET. For P-channel devices, reverse the sign of all voltages and currents.

DC Currents

Note Positive current is current flowing into a terminal.

Ig = gate current = *area*·(Igs + Igd)

Igd = gate-drain leakage current = In + Ir·Kg + Ii

In = normal current = **IS**·$(e^{Vgd/(N \cdot Vt)} - 1)$

Ir = recombination current = **ISR**·$(e^{Vgd/(NR \cdot Vt)} - 1)$

Kg = generation factor = $((1-Vgd/\mathbf{PB})^2 + 0.005)^{\mathbf{M}/2}$

Ii = impact ionization current

For: 0 < Vgs-**VTO** < Vds (forward saturation region)

Ii = Idrain·**ALPHA**·vdif·$e^{-VK/vdif}$

where vdif = Vds - (Vgs-**VTO**)

otherwise

Ii = 0

Id = drain current = *area*·(-Idrain-Igd)

Is = source current = *area*·(Idrain-Igs)

Equation for Idrain

For: Vds ≥ 0 (normal mode)

and: Vgs-**VTO** ≤ 0 (cutoff region)

Idrain = 0

and: Vds ≤ Vgs-**VTO** (linear region)

Idrain = **BETA**·(1+**LAMBDA**·Vds)·Vds·(2·(Vgs-**VTO**)-Vds)

and: 0 < Vgs-**VTO** < Vds (saturation region)

Idrain = **BETA**·(1+**LAMBDA**·Vds)·(Vgs-**VTO**)^2

For: Vds < 0 (inverted mode)

Switch the source and drain in equations (above).

Capacitance

Note All capacitances are between terminals of the intrinsic JFET (that is, to the inside of the ohmic drain and source resistances).

Cgs = gate-source depletion capacitance

For: Vgs ≤ **FC**·**PB**

Cgs = *area*·**CGS**·(1-Vgs/**PB**)$^{-\mathbf{M}}$

For: Vgs > **FC**·**PB**

Cgs = *area*·**CGS**·(1-**FC**)$^{-(1+\mathbf{M})}$·(1-**FC**·(1+**M**)+**M**·Vgs/**PB**)

Cgd = gate-drain depletion capacitance

For: Vgd ≤ **FC**·**PB**

Cgd = *area*·**CGD**·(1-Vgd/**PB**)$^{-\mathbf{M}}$

For: Vgd > **FC**·**PB**

Cgd = *area*·**CGD**·(1-**FC**)$^{-(1+\mathbf{M})}$·(1-**FC**·(1+**M**)+**M**·Vgd/**PB**)

Temperature Effects

VTO(T) = **VTO**+**VTOTC**·(T-Tnom)

BETA(T) = **BETA**·1.01 $^{\textbf{BETA}\text{TCE}\cdot(\text{T-Tnom})}$

IS(T) = **IS**·e $^{(\text{T/Tnom-1})\cdot\text{EG}/(\text{N}\cdot\text{Vt})}$ ·(T/Tnom)$^{\text{XTI/N}}$

where EG = 1.11

ISR(T) = **ISR**·e $^{(\text{T/Tnom-1})\cdot\text{EG}/(\text{NR}\cdot\text{Vt})}$ ·(T/Tnom)$^{\text{XTI/NR}}$

where EG = 1.11

PB(T) = **PB**·T/Tnom - 3·Vt·*ln*(T/Tnom) - Eg(Tnom)·T/Tnom + Eg(T)

where Eg(T) = silicon bandgap energy = 1.16 - .000702·T ^{2} /(T+1108)

CGS(T) = **CGS**·(1+**M**·(.0004·(T-Tnom)+(1-**PB**(T)/**PB**)))

CGD(T) = **CGD**·(1+**M**·(.0004·(T-Tnom)+(1-**PB**(T)/**PB**)))

The drain and source ohmic (parasitic) resistances have no temperature dependence.

Noise

Noise is calculated assuming a one hertz bandwidth, using the following spectral power densities (per unit bandwidth):

the parasitic resistances, Rs and Rd, generate thermal noise ...

Is ^{2} = 4·*k*·T/(**RS**/*area*)

Id ^{2} = 4·*k*·T/(**RD**/*area*)

the intrinsic JFET generates shot and flicker noise ...

Idrain 2 = 4·*k*·T·gm·2/3 + **KF**·Idrain $^{\text{AF}}$ /FREQUENCY

where gm = *d*Idrain/*d*Vgs (at the DC bias point)

Inductor Coupling (transformer core)

General Form

K*<name>* L*<inductor name>* < L*<inductor name>* >*
+ *<coupling value>*

K*<name>* < L*<inductor name>* >* *<coupling value>*
+ *<model name>* *[size value]*

Examples

KTUNED L3OUT L4IN .8

KTRNSFRM LPRIMARY LSECNDRY .99

KXFRM L1 L2 L3 L4 .98 KPOT_3C8

Model Form

.MODEL < *model name*> CORE [*model parameters*]

This device can be used to define coupling between inductors (transformers). This device also refers to a nonlinear magnetic core (CORE) model to include magnetic hysteresis effects in the behavior of a single inductor (winding), or in multiple coupled windings.

Table 2-11 *Inductor Coupling Model Parameters*

Model Parameters*	Description	Units	Default
A	Thermal energy parameter	amp/meter	1E+3
AREA	Mean magnetic cross-section	cm^2	0.1
C	Domain flexing parameter		0.2
GAP	Effective air-gap length	cm	0
K	Domain anisotropy parameter	amp/meter	500
MS	Magnetization saturation	amp/meter	1E+6
PACK	Pack (stacking) factor		1.0
PATH	Mean magnetic path length	cm	1.0

*See .MODEL statement.

Inductor Coupling

K<name> couples two, or more, inductors. Using the “dot” convention, place a “dot” on the first node of each inductor. In other words, given:

```
I1     1    0     AC   1mA
L1     1    0    10uH
L2     2    0    10uH
R2     2    0    .1
K12   L1   L2   .9999
```

the current through L2 is in the opposite direction as the current through L1. The polarity is determined by the order of the nodes in the L device(s) and not by the order of inductors in the K statement.

<coupling value>

This is the “coefficient of mutual coupling” which must be between 0 and 1.
Note that iron-core transformers have a very high coefficient of coupling, greater than .999 in many cases.
For U.C. Berkeley SPICE2: if there are several coils on a transformer, then there must be K statements coupling all combinations of inductor pairs. For instance, a transformer using a center-tapped primary and two secondaries would be written:

```
* PRIMARY
L1   1   2   10uH
L2   2   3   10uH
* SECONDARY
L3   11   12   10uH
L4   13   14   10uH
* MAGNETIC COUPLING
K12   L1   L2   1
K13   L1   L3   1
K14   L1   L4   1
K23   L2   L3   1
K24   L2   L4   1
K34   L3   L4   1
```

This “older” technique is still supported, but **not required**, for simulation. The same transformer can now be written:

```
* PRIMARY
L1 1 2 10uH
L2 2 3 10uH
* SECONDARY
L3 11 12 10uH
L4 13 14 10uH
* MAGNETIC COUPLING
KALL L1 L2 L3 L4 1
```

Note ***Do not mix the two techniques.***

<*model name*>

If < *model name*> is present, four things change:

1. The mutual coupling inductor becomes a nonlinear, magnetic core device. The magnetic core's B-H characteristics are analyzed using the Jiles-Atherton model (see Reference [1] below).
2. The inductors become "windings," so the number specifying inductance now specifies the "number of turns."
3. The list of coupled inductors could be just one inductor.
4. A model statement is required to specify the model parameters.

[*size value*]

Defaults to one and scales the magnetic cross-section. It is intended to represent the number of lamination layers, so only one model statement is needed for each lamination type. For example

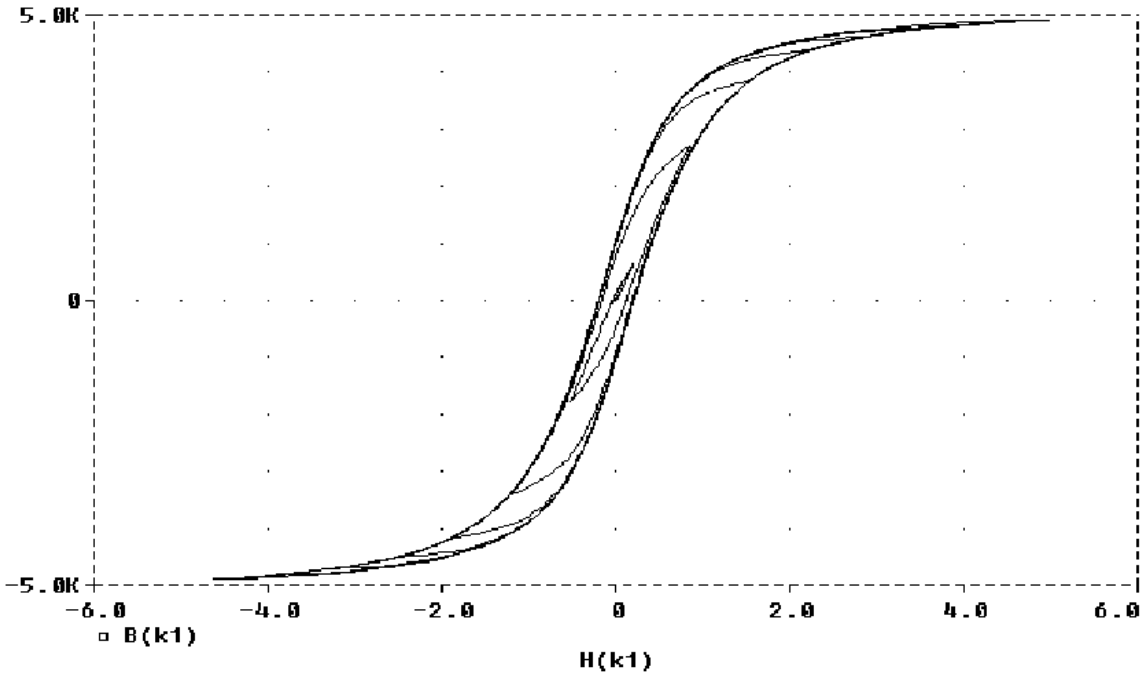
```
L1 5 9 20                       ; inductor having 20 turns
K1 L1 .9999 K528T500_3C8        ; Ferroxcube toroid core
L2 3 8 15                       ; primary winding having 15 turns
L3 4 6 45                       ; secondary winding having 45 turns
K2 L2 L3 .9999 K528T500_3C8     ; another core (not the same as K1)
```

The Jiles-Atherton model is based on existing ideas of domain wall motion, including flexing and translation. The model derives an anhysteric magnetization curve using a mean field technique in which any domain is coupled to the magnetic field (H) and the bulk magnetization (M). This anhysteric value is the magnetization which would be reached in the absence of domain wall pinning. Hysteresis is modeled by the effects of pinning of domain walls on material defect sites. This

impedance to motion and flexing due to the differential field exhibits all of the main features of real, nonlinear magnetic devices, such as: the initial magnetization curve (initial permeability), saturation of magnetization, coercivity, remanence, and hysteresis loss.

These features are shown in Figure 2-4.

Figure 2-4 *Probe B-H display of 3C8 ferrite (Ferroxcube)*



The simulator uses the Jiles-Atherton model to analyze the B-H curve of the magnetic core, and calculate values for inductance and flux for each of the "windings."

The state of the nonlinear core can be viewed in Probe by specifying B(Kxxx), for the magnetization, or H(Kxxx), for the magnetizing influence. These values are not available for .PRINT or .PLOT output.

Reference

For a description of the Jiles-Atherton model, refer to:

[1] D.C. Jiles, and D.L. Atherton, "Theory of ferromagnetic hysteresis," *Journal of Magnetism and Magnetic Materials*, 61, 48 (1986).

Inductor

General Form

L*<name> <(+) node> <(-) node> [model name] <value>*
*+ [*IC*=<initial value>]*

Examples

```
LLOAD   15   0   20mH
L2   1   2   .2E-6
LCHOKE   3   42   LMOD   .03
LSENSE   5   12   2UH     IC=2mA
```

Model Form

.MODEL < *model name*> IND [*model parameters*]

Table 2-12 *Inductor Model Parameters*

Model Parameters*	Description	Units	Default
L	Inductance multiplier		1
IL1	Linear current coefficient	amp^{-1}	0
IL2	Quadratic current coefficient	amp^{-2}	0
TC1	Linear temperature coefficient	$°C^{-1}$	0
TC2	Quadratic temperature coefficient	$°C^{-2}$	0

* see the .MODEL statement

(+) and (-) The (+) and (-) nodes define the polarity when the inductor has a positive voltage across it.

Positive current flows from the (+) node through the inductor to the (-) node.

[*model name*] If [*model name*] is left out, then the effective value is <*value*>.
If [*model name*] is specified, then the effective value is given by the formula

$$<value>\cdot\mathbf{L}\cdot(1+\mathbf{IL1}\cdot\mathbf{I}+\mathbf{IL2}\cdot\mathbf{I}^2)\cdot(1+\mathbf{TC1}\cdot(T\text{-}Tnom)+\mathbf{TC2}\cdot(T\text{-}Tnom)^2)$$

where <*value*> is normally positive (though it can be negative, but **not** zero). “Tnom” is the nominal temperature (set using TNOM option).

<*initial value*> The initial current through the inductor during the bias point calculation.

Noise The inductor does not have a noise model.

MOSFET

General Form

M<*name*> <*drain node*> <*gate node*> <*source node*>
+ <*bulk/substrate node*> <*model name*>
+ [L=<*value*>] [W=<*value*>]
+ [AD=<*value*>] [AS=<*value*>]
+ [PD=<*value*>] [PS=<*value*>]
+ [NRD=<*value*>] [NRS=<*value*>]
+ [NRG=<*value*>] [NRB=<*value*>]
+ [M=<*value*>]

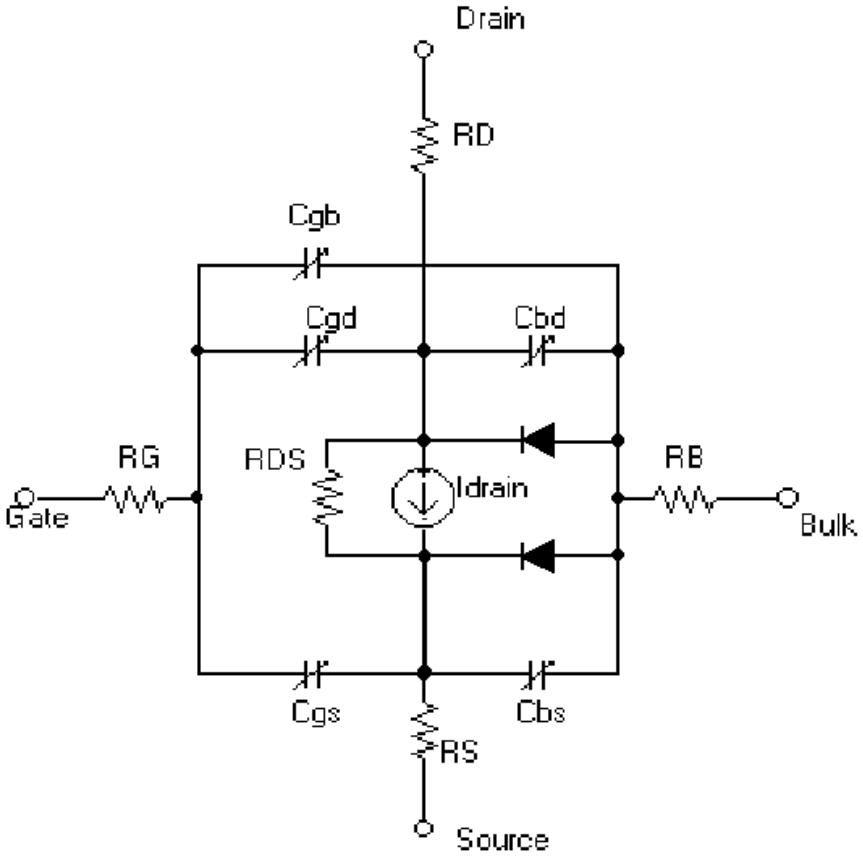
Examples

```
M1   14  2   13  0    PNOM      L=25u   W=12u
M13  15  3    0  0    PSTRONG
M16  17  3    0  0    PSTRONG   M=2
M28   0  2  100 100  NWEAK     L=33u   W=12u
+ AD=288p   AS=288p   PD=60u   PS=60u   NRD=14   NRS=24   NRG=10
```

Model Form

.MODEL < *model name*> NMOS [*model parameters*]
.MODEL < *model name*> PMOS *[model parameters]*

Figure 2-5 *MOSFET Model*



As shown in Figure Model Form, the MOSFET is modeled as an intrinsic MOSFET using ohmic resistances in series with the drain, source, gate, and bulk (substrate). There is also a shunt resistance (RDS) in parallel with the drain-source channel.

The simulator provides four MOSFET device models, which differ in the formulation of the I-V characteristic. The **LEVEL** parameter selects between different models:

Table 2-13 *MOSFET Levels*

MOSFET LEVELS	Model Definition
LEVEL=1	Shichman-Hodges model (see reference [1])
LEVEL=2	geometry-based, analytic model (see reference [2])
LEVEL=3	semi-empirical, short-channel model (see reference [2])
LEVEL=4	BSIM model (see reference [3])

L and W

These are the channel length and width, and are decreased to get the effective channel length and width.

L and W can be specified in the device, model, or .OPTIONS statements. The value in the device statement supersedes the value in the model statement, which supersedes the value in the .OPTIONS statement.

AD and AS

These are the drain and source diffusion areas.

PD and PS

These are the drain and source diffusion perimeters.

The drain-bulk and source-bulk saturation currents can be specified either by **JS**, which is multiplied by AD and AS, or by IS, which is an absolute value. The zero-bias depletion capacitances can be specified by **CJ**, which is multiplied by AD and AS, and by **CJSW**, which is multiplied by PD and PS. Or they can be set by **CBD** and **CBS**, which are absolute values.

NRD, NRS, NRG, and NRB

These are the relative resistivities of the drain, source, gate, and substrate in squares. These parasitic (ohmic) resistances can be specified either by **RSH**, which is multiplied by NRD, NRS, NRG, and NRB respectively or by **RD**, **RS**, **RG**, and **RB**, which are absolute values.

PD and PS default to 0, NRD and NRS default to 1, and NRG and NRB default to 0. Defaults for L, W, AD, and AS can be set in the .OPTIONS statement. If AD or AS defaults are not set, they also default to 0. If L or W defaults are not set, they default to 100u.

M Device “multiplier” (default = 1), which simulates the effect of multiple devices in parallel.

The effective width, overlap and junction capacitances, and junction currents of the MOSFET are multiplied by M. The parasitic resistance values (e.g., **RD** and **RS**) are divided by M. Note the third example showing a device twice the size of the second example.

Model Levels 1, 2, and 3

The DC characteristics of the first three model levels are defined by the parameters **VTO**, **KP**, **LAMBDA**, **PHI**, and **GAMMA**. These are computed by the simulator if process parameters (e.g., **TOX**, and **NSUB**) are given, but the user-specified values always override (**Note**: The default value for **TOX** is 0.1 μ for model levels two and three, but is unspecified for level one which “turns off” the use of process parameters). **VTO** is positive (negative) for enhancement mode and negative (positive) for depletion mode of N-channel (P-channel) devices.

Table 2-14 *MOSFET Level 1, 2, and 3 Model Parameters*

Model Parameters*	Description	Units	Default
DELTA	Width effect on threshold		0
ETA	Static feedback (**LEVEL**=3)		0
GAMMA	Bulk threshold parameter	$volt^{1/2}$	calculated
KP	Transconductance coefficient	$amp/volt^2$	2E-5
KAPPA	Saturation field factor (**LEVEL**=3)		0.2
LAMBDA	Channel-length modulation (**LEVEL**=1 or 2)	$volt^{-1}$	0
LD	Lateral diffusion (length)	meter	0
NEFF	Channel charge coefficient (**LEVEL**=2)		1.0
NFS	Fast surface state density	$1/cm^2$	0
NSS	Surface state density	$1/cm^2$	none
NSUB	Substrate doping density	$1/cm^3$	none
PHI	Surface potential	volt	0.6
THETA	Mobility modulation (**LEVEL**=3)	$volt^{-1}$	0
TOX	Oxide thickness	meter	see above
TPG	Gate material type: +1 = opposite of substrate -1 = same as substrate 0 = aluminum +1		+1
UCRIT	Mobility degradation critical field (**LEVEL**=2)	volt/cm	1E4
UEXP	Mobility degradation exponent (**LEVEL**=2)		0
UTRA	(*not used*) Mobility degradation transverse field coefficient		0
UO	Surface mobility. (The second character is the letter O, not the numeral zero.)	$cm^2/volt \cdot sec$	600
VMAX	Maximum drift velocity	meter/sec	0
VTO	Zero-bias threshold voltage	volt	0
WD	Lateral diffusion (width)	meter	0
XJ	Metallurgical junction depth (**LEVEL**=2 or 3)	meter	0
XQC	Fraction of channel charge attributed to drain		1.0

* See .MODEL statement.

Model Level 4

The **LEVEL**=4 (BSIM1) model parameters are all values obtained from process characterization, and can be generated automatically. Reference [4] describes a means of generating a "process" file, which mut then be converted into .MODEL statements for inclusion in the Model Library or circuit file. (The simulator does not read process files.)

In the following list, parameters marked using a "ζ" in the L&W column also have corresponding parameters with a length and width dependency. For example, VFB is a basic parameter using units of volts, and LVFB and WVFB also exist and have units of volt·μ. The formula

$$P_i = P_0 + P_L/L_e + P_w/W_e$$

is used to evaluate the parameter for the actual device, where

L_e = effective length = L - DL

W_e = effective width = W - DW

Note ***Unlike the other models in PSpice, the BSIM model is designed for use with a process characterization system that provides all parameters: there are no defaults specified for the parameters, and leaving one out can cause problems.***

Table 2-15 *MOSFET Level 4 Model Parameters*

Model Parameters*	Description	Units	L&W
DELL	Drain, source junction length reduction	meter	
DL	Channel shortening	μ	
DW	Channel narrowing	μ	
ETA	Zero-bias drain-induced barrier lowering coefficient		ζ
K1	Body effect coefficient	$volt^{½}$	ζ
K2	Drain/source depletion charge sharing coefficient		ζ
MUS	Mobility at zero substrate bias and Vds=Vdd	$cm^2/v^2 \cdot sec$	ζ

MUZ	Zero-bias mobility	$cm^2/v \cdot sec$	
N0	Zero-bias subthreshold slope coefficient		ζ
NB	Sens. of subthreshold slope to substrate bias		ζ
ND	Sens. of subthreshold slope to drain bias		ζ
PHI	Surface inversion potential	volt	ζ
TEMP	Temperature at which parameters were measured	°C	
TOX	Gate-oxide thickness	μ	
U0	Zero-bias transverse-field mobility degradation	$volt^{-1}$	ζ
U1	Zero-bias velocity saturation	μ/volt	ζ
VDD	Measurement bias range	volts	
VFB	Flat-band voltage	volt	ζ
WDF	Drain, source junction default width	meter	
X2E	Sens. of drain-induced barrier lowering effect to substrate bias	$volt^{-1}$	ζ
X2MS	Sens. of mobility to substrate bias @ Vds=0	$cm^2/v^2 \cdot sec$	ζ
X2MZ	Sens. of mobility to substrate bias @ Vds=0	$cm^2/v^2 \cdot sec$	ζ
X2U0	Sens. of transverse-field mobility degradation effect to substrate bias	$volt^{-2}$	ζ
X2U1	Sens. of velocity saturation effect to substrate bias	$\mu/volt^2$	ζ
X3E	Sens. of drain-induced barrier lowering effect to drain bias @ Vds = Vdd	$volt^{-1}$	ζ
X3MS	Sens. of mobility to drain bias @ Vds=Vdd	$cm^2/v^2 \cdot sec$	ζ
X3U1	Sens. of velocity saturation effect on drain	$\mu/volt^2$	ζ
XPART	Gate-oxide capacitance charge model flag. **XPART**=0 selects a 40/60 drain/source charge partition in saturation, while **XPART**=1 selects a 0/100 drain/source charge partition.		

***See .MODEL statement**

ζ in L&W column indicates that parameter may have corresponding parameters exhibiting length and width dependence. See discussion under Model Level 4 on page 2-40.

For All Model Levels

The following list describes the parameters common to all model levels, which are primarily parasitic element values such as series resistance, overlap and junction capacitance, and so on.

Table 2-16 *MOSFET Model Parameters for All Levels*

Model Parameters*	Description	Units	Default
AF	Flicker noise exponent		1
CBD	Zero-bias bulk-drain *p-n* capacitance	farad	0
CBS	Zero-bias bulk-source *p-n* capacitance	farad	0
CGBO	Gate-bulk overlap capacitance/channel length	farad/meter	0
CGDO	Gate-drain overlap capacitance/channel width	farad/meter	0
CGSO	Gate-source overlap capacitance/channel width	farad/meter	0
CJ	Bulk *p-n* zero-bias bottom capacitance/area	farad/meter^2	0
CJSW	Bulk *p-n* zero-bias sidewall capacitance/length	farad/meter	0
FC	Bulk *p-n* forward-bias capacitance coefficient		0.5
IS	Bulk *p-n* saturation current	amp	1E-14
JS	Bulk *p-n* saturation current/area	amp/meter^2	0
JSSW	Bulk *p-n* saturation sidewall current/length	amp/meter	0
KF	Flicker noise coefficient		0
L	Channel length	meter	**DEFL**
LEVEL	Model index		1
MJ	Bulk *p-n* bottom grading coefficient		0.5
MJSW	Bulk *p-n* sidewall grading coefficient		0.33
N	Bulk *p-n* emission coefficient		1
PB	Bulk *p-n* bottom potential	volt	0.8
PBSW	Bulk *p-n* sidewall potential	volt	**PB**
RB	Bulk ohmic resistance	ohm	0
RD	Drain ohmic resistance	ohm	0
RDS	Drain-source shunt resistance	ohm	infinite
RG	Gate ohmic resistance	ohm	0
RS	Source ohmic resistance	ohm	0
RSH	Drain, source diffusion sheet resistance	ohm/square	0
TT	Bulk *p-n* transit time	sec	0
W	Channel width	meter	**DEFW**

Equations

In the following equations:

Vgs = intrinsic gate-intrinsic source voltage

Vgd = intrinsic gate-intrinsic drain voltage

Vds = intrinsic drain-intrinsic source voltage

Vbs = intrinsic substrate-intrinsic source voltage

Vbd = intrinsic substrate-intrinsic drain voltage

Vt = $k \cdot T/q$ (thermal voltage)

k = Boltzmann's constant

q = electron charge

T = analysis temperature (°K)

Tnom = nominal temperature (set using TNOM option)

Other variables are from the model parameter list. These equations describe an N-channel MOSFET. For P-channel devices, reverse the signs of all voltages and currents. Positive current is current flowing into a terminal (for example, positive drain current flows from the drain through the channel to the source).

DC Currents [1]

Ig = gate current = 0

Ib = bulk current = Ibs+Ibd

Ibs = bulk-source leakage current = $Iss \cdot (e^{Vbs/(N \cdot Vt)} - 1)$

Ibd = bulk-drain leakage current = $Ids \cdot (e^{Vbd/(N \cdot Vt)} - 1)$

where if: **JS** = 0, or AS = 0, or AD = 0

Iss = IS

Ids = IS

otherwise:

Iss = AS·**JS** + PS·**JSSW**

Ids = AD·**JS** + PD·**JSSW**

Id = drain current = -Idrain+Ibd

Is = source current = Idrain+Ids

Equations for Idrain: LEVEL=1

For: Vds ≥ 0 (normal mode)

and: Vgs-V_{to} < 0 (cutoff region)

Idrain = 0

and: Vds < Vgs-V_{to} (linear region)

Idrain = (W/L)·(**KP**/2)·(1+**LAMBDA**·Vds)·Vds·(2·(Vgs-V_{to})-Vds)

and: 0 ≤ Vgs-V_{to} ≤ Vds (saturation region)

Idrain = (W/L)·(**KP**/2)·(1+**LAMBDA**·Vds)·(Vgs-V_{to})^2

where V_{to} = **VTO** + **GAMMA**·((**PHI**-Vbs)$^{1/2}$ -**PHI**$^{1/2}$)

For: Vds < 0 (inverted mode)

Switch the source and drain in equations (above).

For **LEVEL**=2, or **LEVEL**=3 MOSFET models, see reference [2] on 2-30 for detailed information.

1. Positive current is current flowing into a terminal.

Capacitance[1]

Cbs = bulk-source capacitance = area cap. + sidewall cap. + transit time cap.

Cbd = bulk-drain capacitance = area cap. + sidewall cap. + transit time cap.

For: **CBS** = 0 and **CBD** = 0

Cbs = AS·**CJ**·Cbsj + PS·**CJSW**·Cbss + **TT**·Gbs

Cbd = AD·**CJ**·Cbdj + PD·**CJSW**·Cbds + **TT**·Gds

otherwise

Cbs = **CBS**·Cbsj + PS·**CJSW**·Cbss + **TT**·Gbs

Cbd = **CBD**·Cbdj + PD·**CJSW**·Cbds + **TT**·Gds

where

Gbs = DC bulk-source conductance = *d*Ibs/*d*Vbs

Gbd = DC bulk-drain conductance = *d*Ibd/*d*Vbd

or: Vbs ≤ **FC·PB**

Cbsj = (1-Vbs/**PB**) $^{-MJ}$

Cbss = (1-Vbs/**PBSW**) $^{-MJSW}$

For: Vbs > **FC**·**PB**

Cbsj = (1-**FC**) $^{-(1+MJ)}$ ·(1-**FC**·(1+**MJ**)+**MJ**·Vbs/**PB**)

Cbss = (1-**FC**) $^{-(1+MJSW)}$ ·(1-**FC**·(1+**MJSW**)+**MJSW**·Vbs/**PBSW**)

For: Vbd ≤ **FC**·**PB**

Cbdj = (1-Vbd/**PB**) $^{-MJ}$

Cbds = (1-Vbd/**PBSW**) $^{-MJSW}$

For: Vbd > **FC**·**PB**

Cbdj = (1-**FC**) $^{-(1+MJ)}$ ·(1-**FC**·(1+**MJ**)+**MJ**·Vbd/**PB**)

Cbds = (1-**FC**) $^{-(1+MJSW)}$ ·(1-**FC**·(1+**MJSW**)+**MJSW**·Vbd/**PBSW**)

Cgs = gate-source overlap capacitance = **CGSO**·W

Cgd = gate-drain overlap capacitance = **CGDO**·W

Cgb = gate-bulk overlap capacitance = **CGBO**·L

See reference [2] for the equations describing the capacitances due to the channel charge.

1. All capacitances are between terminals of the intrinsic MOSFET. That is, to the inside of the ohmic drain and source resistances.

Temperature Effects

IS(T) = **IS**·$e^{(Eg(Tnom)\cdot T/Tnom - Eg(T))/V_t}$

JS(T) = **JS**·$e^{(Eg(Tnom)\cdot T/Tnom - Eg(T))/V_t}$

JSSW(T) = **JSSW**·$e^{(Eg(Tnom)\cdot T/Tnom - Eg(T))/V_t}$

PB(T) = **PB**·T/Tnom - 3·Vt·*ln*(T/Tnom) - Eg(Tnom)·T/Tnom + Eg(T)

PBSW(T) = **PBSW**·T/Tnom - 3·Vt·*ln*(T/Tnom) - Eg(Tnom)·T/Tnom + Eg(T)

PHI(T) = **PHI**·T/Tnom - 3·Vt·*ln*(T/Tnom) - Eg(Tnom)·T/Tnom + Eg(T)

where Eg(T) = silicon bandgap energy = 1.16 - .000702·T^2/(T+1108)

CBD(T) = **CBD**·(1+**MJ**·(.0004·(T-Tnom)+(1-**PB**(T)/**PB**)))

CBS(T) = **CBS**·(1+**MJ**·(.0004·(T-Tnom)+(1-**PB**(T)/**PB**)))

CJ(T) = **CJ**·(1+MJ·(.0004·(T-Tnom)+(1-**PB**(T)/**PB**)))

CJSW(T) = **CJSW**·(1+**MJSW**·(.0004·(T-Tnom)+(1-**PB**(T)/**PB**)))

KP(T) = **KP**·$(T/Tnom)^{-3/2}$

UO(T) = **UO**·$(T/Tnom)^{-3/2}$

MUS(T) = **MUS**·$(T/Tnom)^{-3/2}$

MUZ() = **MUZ**·(T/Tnom)$^{-3/2}$

X3MS(T) = **X3MS**·(T/Tnom)$^{-3/2}$

The ohmic (parasitic) resistances have no temperature dependence.

Noise

Noise is calculated assuming a one hertz bandwidth, using the following spectral power densities (per unit bandwidth):

the parasitic resistances (Rd, Rg, Rs, and Rb) generate thermal noise ...

$Id^2 = 4 \cdot k \cdot T/Rd$

$Ig^2 = 4 \cdot k \cdot T/Rg$

$Is^2 = 4 \cdot k \cdot T/Rs$

$Ib^2 = 4 \cdot k \cdot T/Rb$

the intrinsic MOSFET generates shot and flicker noise ...

$Idrain^2 = 4 \cdot k \cdot T \cdot gm \cdot 2/3 + \mathbf{KF} \cdot Idrain^{AF}/(FREQUENCY \cdot Kchan)$

where

gm = *d*Idrain/*d*Vgs (at the DC bias point)

Kchan = (effective length) ^{2}·(permittivity of SiO_2)/**TOX**

References

For a more complete description of the MOSFET models, refer to:

[1] H. Shichman and D. A. Hodges, "*Modeling and simulation of insulated-gate field-effect transistor switching circuits*," IEEE Journal of Solid-State Circuits, SC-3, 285, September 1968.

[2] A. Vladimirescu, and S. Lui, "*The Simulation of MOS Integrated Circuits Using SPICE2*," Memorandum No. M80/7, February 1980.

[3] B. J. Sheu, D. L. Scharfetter, P.-K. Ko, and M.-C. Jeng, "*BSIM: Berkeley Short-Channel IGFET Model for MOS Transistors*," IEEE Journal of Solid-State Circuits, SC-22, 558-566, August 1987.

[4] J. R. Pierret, "*A MOS Parameter Extraction Program for the BSIM Model*," Memorandum No. M84/99 and M84/100, November 1984.

Digital Input

General Form

N<*name*> <*interface node*> <*low level node*> <*high level node*>
+ <*model name*>
+ DGTLNET = <*digital net name*>
+ <*digital I/O model name*>
+ SIGNAME=<*digital signal name*>
+ [IS = *initial state*]

Example

```
NRESET   7   15   16   FROM_TTL
N12      18   0 100   FROM_CMOS  SIGNAME=VCO_GATE   IS=0
```

Model Form

.MODEL < *model name*> DINPUT [*model parameters*]

Table 2-17 *Digital Input Model Parameters*

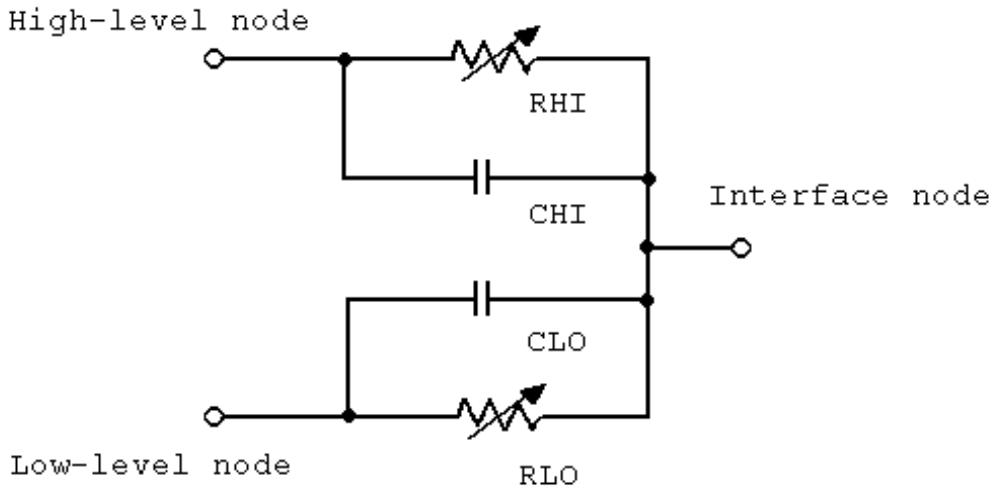
Model Parameters*	Description	Units	Default
CHI	Capacitance to high level node	farad	0
CLO	Capacitance to low level node	farad	0
FILE	Digital input file name (Digital Files only)		
FORMAT	Digital input file format (Digital Files only)		1
S0NAME	State “0” character abbreviation		
S0TSW	State “0” switching time	sec	
S0RLO	State “0” resistance to low level node	ohm	
S0RHI	State “0” resistance to high level node	ohm	
S1NAME	State “1” character abbreviation		
S1TSW	State “1” switching time	sec	
S1RLO	State “1” resistance to low level node	ohm	
S1RHI	State “1” resistance to high level node	ohm	
S2NAME	State “2” character abbreviation		
S2TSW	State “2” switching time	sec	
S2RLO	State “2” resistance to low level node	ohm	
S2RHI	State “2” resistance to high level node	ohm	
..	.		
S19NAME	State “19” character abbreviation		
S19TSW	State “19” switching time	sec	
S19RLO	State “19” resistance to low level node	ohm	
S19RHI	State “19” resistance to high level node	ohm	
TIMESTEP	Digital input file step-size (Digital Files only)	sec	1E-91

* See .MODEL statement.

Note *For more information on using the digital input device to simulate mixed analog/digital systems refer to your PSpice user's guide.*

As shown in Figure 2-6, the digital input device is modeled as a time varying resistor from <*low level node*> to <*interface node*>, and another time varying resistor from <*high level node*> to <*interface node*>. Each of these resistors has an optional fixed value capacitor in parallel: CLO and CHI. When the state of the digital signal changes, the values of the resistors change (exponentially) from their present values to the values specified for the new state over the switching time specified by the new state. Normally the low and high level nodes would be attached to voltage sources which would correspond to the highest and lowest logic levels. (Using two resistors and two voltage levels, any voltage between the two levels can be created at any impedance.

Figure 2-6 *Digital Input Model*



If SIGNAME = <*digital signal name*> is specified, this is the name of the digital signal in the input file which controls this digutal input device. Otherwise, the portion of the device name after the leading N identifies the name of the digital signal.

If IS=<*initial state name*> is specified, then the initial state of the input (for the bias-point calculation, and TIME=0) is **not the value specified** by the input file (or the digital simulator) but the value specified by <*initial state*>. The digital input will remain in this state until a value is read, or received, which is different than the state at TIME=0. The value of <*initial state*> must be one of the state names (S0NAME through S19NAME) specified by the model.

The state of the digital input may be viewed in *Probe* by specifying B(Nxxx). The value of B(Nxxx) is 0.0 if the current state is S0NAME, 1.0 if the current state is S1NAME, and so on through 19.0. For this reason it is convenient to use S0NAME for the lowest logic level, and S19NAME for the highest logic level. These values are not available for .PRINT or .PLOT output. If the file name Is DGTLPSPC, and the *Parallel Analog/Digital Simulation* option in included, then *Pspice* will obtain the digital input data from the digital simulator (for example, VIEW*sim*A/D). In this case the digital simulator must be running concurrently with *Pspice*, and they must both be simulating the same time interval.

The format parameter is ignored if DGTLPSPC is specified for the file.

Any number of digital input models may be specified. Different digital input models may reference the same file, or different files. (If the models reference the same file, the file must be specified in the same way, or unpredictable results will occur: for example, if the default drive is C:, then one model should not have FILE=C:TEST.DAT if another has FILE=TEST.DAT).

Digital Output

General Form

O<*name*> <*interface node*> <*reference node*> <*model name*>
\+ [DGTLNET = <*digital I/O model name*>]
\+ [SIGNAME = <*digital signal name*>]

Example

```
OVCO  17   0  TO_TTL
O5    22 100  TO_CMOS    SIGNAME=VCO_OUT
```

Table 2-18 *Digital Output Model Parameters*

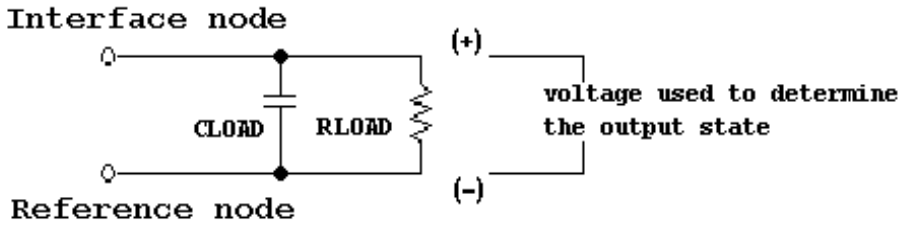
Model Parameters *	Description	Units	Default
CHGONLY	0: write each timestep, 1: write upon change 0		
CLOAD	Output capacitor	farad	0
FILE	Digital input file name (Digital Files only)		
FORMAT	Digital input file format (Digital Files only)		1
RLOAD	Output resistor	ohm	1000
S0NAME	State “0” character abbreviation		
S0VLO	State “0” low level voltage	volt	
S0VHI	State “0” high level voltage	volt	
S1NAME	State “1” character abbreviation		
S1VLO	State “1” low level voltage	volt	
S1VHI	State “1” high level voltage	volt	
S2NAME	State “2” character abbreviation		
S2VLO	State “2” low level voltage	volt	
S2VHI	State “2” high level voltage	volt	
.	.		
S19NAME	State “19” character abbreviation		
S19VLO	State “19” low level voltage	volt	
S19VHI	State “19” high level voltage	volt	
TIMESTEP	Digital input file step-size	sec	1E-9
TIMESCALE	Scale factor for TIMESTEP (Digital Files only)		1

- See .MODEL statement

Note The digital output device is part of the mixed analog/digital simulation options for *Pspice*. For more information see the “Digital Files” chapter.

As shown in Figure 2-7, the digital output device is modeled as a resistor and capacitor, of the values specified in the model statement, connected between <*interface node*> and <*reference node*>. At times which are integer multiples of TIMESTEP, the “state” of the device node is determined and written to the specified file.

Figure 2-7 *Digital Output Model*



The state of the node is determined by taking the difference in voltage between the <*interface node*> and the <*reference node*>, and comparing it (first) to the voltage range for the current state. If it is within the range, then the new state is the same as the old state. If it is not within the range for the current state, then the states are examined starting with S0NAME. The new state is the first one which contains the voltage within its range. (If none contain it, then the state is ‘?’). This allows the user to specify hysteresis for the state changes.

If SIGNAME = <*digital signal name*> is specified, this is the name of the digital signal in the output file. Otherwise, the portion of the device name after the leading O identifies the name of the digital signal.

The state of each device will be written to the output file at times which are integer multiples of TIMESTEP. The “time” which is written will be the integer

time = TIMESCALE * TIME/TIMESTEP

TIMESCALE defaults to 1, but if the digital simulator is using a very small timestep compared to the *Pspice* timestep, it can speed up the *Pspice* simulation to increase the value of both TIMESTEP and TIMESCALE. This is because *Pspice* must take time-steps no greater than the digital TIMESTEP size when a digital output is about to change, in order to accurately determine the exact time that the state changes. The value of TIMESTEP should therefore be the time resolution required at the analog-digital interface. The value of TIMESCALE is then used to adjust the output time to be in the same units as the digital simulator uses. For example, if you are doing a digital simulation with a timestep of 100ps, but your circuit has a clock rate of 1us, setting TIMESTEP to 0.1us should provide enough resolution. Setting TIMESCALE to 1000 will scale the output time to be in 100ps units.

If CHGONLY=1 only those time-steps in which an digital output state changes are written to the file.

The state of the digital output may be viewed in *Probe* by specifying B(Oxxx). The value of B(Oxxx) is 0.0 if the current state is S0NAME, 1.0 if the current state is S1NAME, and so on through 19.0. For this reason it is convenient to use S0NAME for the lowest logic level, and S19NAME for the highest logic level. These values are not available for .PRINT or .PLOT output.

If the file name is PSPCDGTL, and the *Parallel Analog/Digital Simulation* option in included, then *Pspice* will obtain the digital input data from the digital simulator (for example, VIEW*sim*A/D). In this case the digital simulator must be running concurrently with *Pspice*, and they must both be

simulating the same time interval. The format parameter is ignored if PSPCGTL is specified for the file.

Any number of digital output models may be specified. Different digital input models may reference the same file, or different files. (If the models reference the same file, the file must be specified in the same way, or unpredictable results will occur: for example, if the default drive is C:, then one model should not have FILE=C:TEST.DAT if another has FILE=TEST.DAT).

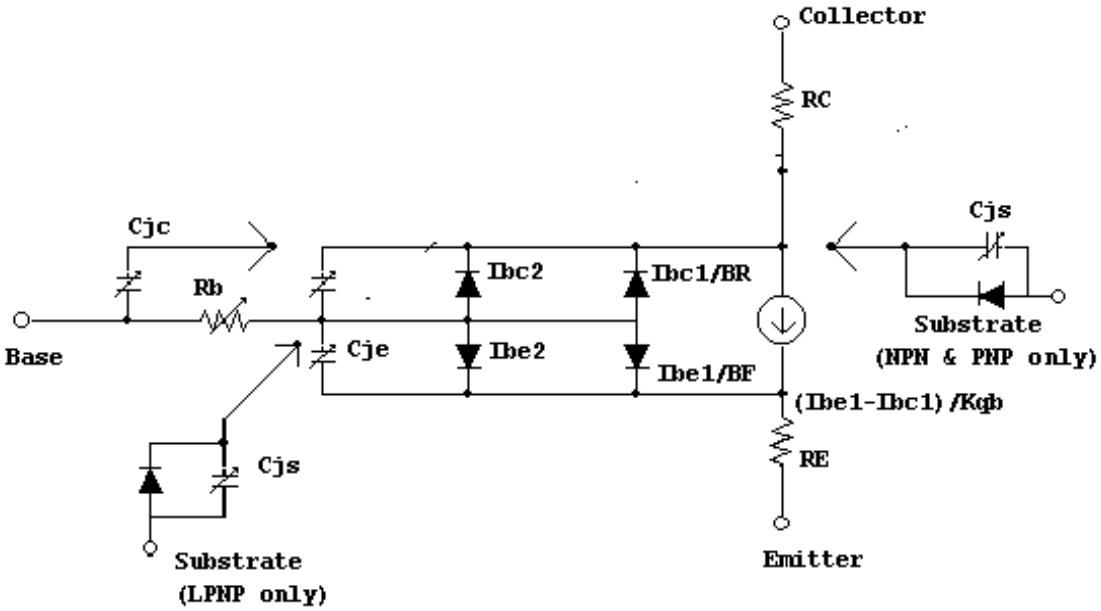
Bipolar Transistor

General Form Q<*name*> < *collector node*> <*base node*> <*emitter node*>
+ [*substrate node*] <*model name*> [*area value*]

Examples
Q1 14 2 13 PNPNOM
Q13 15 3 0 1 NPNSTRONG 1.5
Q7 VC 5 12 [SUB] LATPNP

Model Form
.MODEL < model name> NPN [model parameters]
.MODEL < model name> PNP [model parameters]
.MODEL < model name> LPNP [model parameters]

Figure 2-8 *Bipolar Transistor Model (enhanced Gummel-Poon)*



As shown, the bipolar transistor is modeled as an intrinsic transistor using ohmic resistances in series with the collector (RC/*area*), the base (value varies with current, see equations below), and with the emitter (RE/*area*). Positive current is current flowing into a terminal. The [*area value*] is the relative device area and defaults to 1. For those model parameters which have alternate names, such as VAF and VA (the alternate name is shown by using parentheses), either name can be used.

The substrate node is optional, and if not specified it defaults to ground. Because the simulator allows alphanumeric names for nodes, and because there is no easy way to distinguish these from the model names, it makes it necessary to enclose the name (not a number) used for the substrate node using square brackets “[ ]”. Otherwise it is interpreted as a model name. See the third example.

For model types NPN and PNP, the isolation junction capacitance is connected between the intrinsic-collector and substrate nodes. This is the same as in SPICE2, or SPICE3, and works well for vertical IC transistor structures. For lateral IC transistor structures there is a third model, LPNP, where the isolation junction capacitance is connected between the intrinsic-base and substrate nodes.

Table 2-19 *Bipolar Transistor Model Parameters*

Model Parameters	Description	Units	Default
AF	Flicker noise exponent		1
BF	Ideal maximum forward beta		100
BR	Ideal maximum reverse beta		1
CJC	Base-collector zero-bias *p-n* capacitance	farad	0
CJE	Base-emitter zero-bias *p-n* capacitance	farad	0
CJS(CCS)	Substrate zero-bias *p-n* capacitance	farad	0
EG	Bandgap voltage (barrier height)	eV	1.11
FC	Forward-bias depletion capacitor coefficient		0.5
IKF (IK)	Corner for forward-beta high-current roll-off	amp	infinite
IKR	Corner for reverse-beta high-current roll-off	amp	infinite
IRB	Current at which Rb falls halfway to RBM	amp	infinite
IS	Transport saturation current	amp	1E-16
ISC (C4)	Base-collector leakage saturation current	amp	0
ISE (C2)	Base-emitter leakage saturation current	amp	0
ISS	Substrate *p-n* saturation current	amp	0
ITF	Transit time dependency on Ic	amp	0
KF	Flicker noise coefficient		0
MJC (MC)	Base-collector *p-n* grading factor		0.33
MJE (ME)	Base-emitter *p-n* grading factor		0.33
MJS (MS)	Substrate *p-n* grading factor		0
NC	Base-collector leakage emission coefficient		2

Table 2-19 *Bipolar Transistor Model Parameters (continued)*

Model Parameters	Description	Units	Default
NE	Base-emitter leakage emission coefficient		1.5
NF	Forward current emission coefficient		1
NR	Reverse current emission coefficient		1
NS	Substrate *p-n* emission coefficient		1
PTF	Excess phase @ 1/(2p·TF)Hz	degree	0
QCO	Epitaxial region charge factor	coulomb	0
RB	Zero-bias (maximum) base resistance	ohm	0
RBM	Minimum base resistance	ohm	RB
RC	Collector ohmic resistance	ohm	0
RE	Emitter ohmic resistance	ohm	0
TF	Ideal forward transit time	sec	0
TR	Ideal reverse transit time	sec	0
TRB1	RB temperature coefficient (linear)	$°C^{-1}$	0
TRB2	RB temperature coefficient (quadratic)	$°C^{-2}$	0
TRC1	RC temperature coefficient (linear)	$°C^{-1}$	0
TRC2	RC temperature coefficient (quadratic)	$°C^{-2}$	0
TRE1	RE temperature coefficient (linear)	$°C^{-1}$	0
TRE2	RE temperature coefficient (quadratic)	$°C^{-2}$	0
TRM1	RBM temperature coefficient (linear)	$°C^{-1}$	0
TRM2	RBM temperature coefficient (quadratic)	$°C^{-2}$	0
VAF (VA)	Forward Early voltage	volt	infinite
VAR (VB)	Reverse Early voltage	volt	infinite
VJC (PC)	Base-collector built-in potential	volt	0.75
VJE (PE)	Base-emitter built-in potential	volt	0.75
VJS (PS)	Substrate *p-n* built-in potential	volt	0.75
VTF	Transit time dependency on Vbc	volt	infinite
XCJC	Fraction of CJC connec. internally to Rb		1
XTB	Forward and reverse beta temp coeff.		0
XTF	Transit time bias dependence coefficient		0
XTI (PT)	IS temperature effect exponent		3

The parameters ISE (C2) and ISC (C4) can be set to be greater than one. In this case, they are interpreted as multipliers of IS instead of absolute currents: that is, if ISE is greater than one then it is replaced by ISE·IS. Likewise for ISC.

Equations

In the following equations:

Vbe = intrinsic base-intrinsic emitter voltage
Vbc = intrinsic base-intrinsic collector voltage
Vbs = intrinsic base-substrate voltage
Vbx = extrinsic base-intrinsic collector voltage
Vce = intrinsic collector-intrinsic emitter voltage
Vjs = (NPN) intrinsic collector-substrate voltage
= (PNP) intrinsic substrate-collector voltage
= (LPNP) intrinsic base-substrate voltage
Vt = k·T/q (thermal voltage)
k = Boltzmann's constant
q = electron charge
T = analysis temperature (°K)
Tnom = nominal temperature (set using TNOM option)

Other variables are from the model parameter list. These equations describe an NPN transistor. For the PNP and LPNP devices, reverse the signs of all voltages and currents.

DC Currents

Note: Positive current is current flowing into a terminal.

Ib = base current = *area*·(Ibe1/**BF** + Ibe2 + Ibc1/**BR** + Ibc2)

Ic = collector current = *area*·(Ibe1/Kqb - Ibc1/Kqb - Ibc1/**BR** - Ibc2)

Ibe1 = forward diffusion current = **IS**·$(e^{Vbe/(NF\cdot Vt)}-1)$

Ibe2 = non-ideal base-emitter current = **ISE**·$(e^{Vbe/(NE\cdot Vt)}-1)$

Ibc1 = reverse diffusion current = **IS**·$(e^{Vbc/(NR\cdot Vt)}-1)$

Ibc2 = non-ideal base-collector current = **ISC**·$(e^{Vbc/(NC\cdot Vt)}-1)$

Kqb = base charge factor = Kq1·$(1+(1+4\cdot Kq2)^{1/2})/2$

Kq1 = 1/(1 - Vbc/**VAF** - Vbe/**VAR**)

Kq2 = Ibe1/**IKF** + Ibc1/**IKR**

Is = substrate current = *area*·ISS·$(e^{Vjs/(NS\cdot Vt)}-1)$

Rb = actual base parasitic resistance

For: **IRB** = infinite (default value)

Rb = (**RBM** + (**RB**-**RBM**)/Kqb)/*area*

For: **IRB** > 0

$Rb = (\mathbf{RBM} + 3\cdot(\mathbf{RB}-\mathbf{RBM})\cdot(tan(x)-x)/(x\cdot tan^2(x)))/area$

where $x = ((1+(144/\pi^2)\cdot Ib/(area\cdot \mathbf{IRB}))^{1/2} -1)/ ((24/\pi^2)\cdot(Ib/(area\cdot \mathbf{IRB}))^{1/2})$

Capacitances

Note: All capacitances, except Cbx, are between terminals of the intrinsic transistor which is inside of the col-lector, base, and emitter parasitic resistances. Cbx is between the intrinsic collector and the extrinsic base.

Cbe = base-emitter capacitance = *area*·(Ctbe + Cjbe)

Ctbe = transit time capacitance = tf·Gbe

tf = effective **TF**= **TF**·(1+**XTF**·($3x^2$-$2x^3$)·$e^{Vbc/(1.44\cdot VTF)}$)

where x= Ibe1/(Ibe1+*area*·**ITF**)

Gbe = DC base-emitter conductance = (*d*Ibe1)/(*d*Vbe)

For: Vbe ≤ **FC**·**VJE**

Cjbe = **CJE**·(1-Vbe/**VJE**)$^{-MJE}$

For: Vbe > **FC**·**VJE**

Cjbe = **CJE**·(1-**FC**)$^{-(1+MJE)}$·(1-**FC**·(1+**MJE**)+**MJE**·Vbe/**VJE**)

Cbc = base-collector capacitance = *area*·(Ctbc+**XCJC**·Cjbc)

Ctbc = transit time capacitance = **TR**·Gbc

Gbc = DC base-collector conductance = (*d*Ibc)/(*d*Vbc)

For: Vbc ≤ **FC**·**VJC**

Cjbc = **CJC**·(1-Vbc/**VJC**)$^{-MJC}$

For: Vbc > **FC**·**VJC**

Cjbc = **CJC**·(1-**FC**)$^{-(1+MJC)}$·(1-**FC**·(1+**MJC**)+**MJC**·Vbc/**VJC**)

Cbx = extrinsic-base to intrinsic-collector capacitance = *area*·(1-**XCJC**)·Cjbx

For: Vbx ≤ **FC**·**VJC**

Cjbx = **CJC**·(1-Vbx/**VJC**)$^{-MJC}$

For: Vbx > **FC**·**VJC**

Cjbx = **CJC**·(1-**FC**)$^{-(1+MJC)}$·(1-**FC**·(1+**MJC**)+**MJC**·Vbx/**VJC**)

Cjs = substrate junction capacitance = *area*·Cjjs

For: Vjs ≤ 0

Cjjs = **CJS**·(1-Vjs/**VJS**)$^{-MJS}$ (assumes **FC** = 0)

For: Vjs > 0

Cjjs = **CJS**·(1+**MJS**·Vjs/**VJS**)

Temperature Effects

$$\mathbf{IS}(T) = \mathbf{IS}\cdot e^{(T/Tnom-1)\cdot EG/(N\cdot Vt)}\cdot(T/Tnom)^{XTI/N}$$

where N = 1

$$\mathbf{ISE}(T) = (\mathbf{ISE}/(T/Tnom)^{XTB})\cdot e^{(T/Tnom-1)\cdot EG/(NE\cdot Vt)}\cdot(T/Tnom)^{XTI/NE}$$

$$\mathbf{ISC}(T) = (\mathbf{ISC}/(T/Tnom)^{XTB})\cdot e^{(T/Tnom-1)\cdot EG/(NC\cdot Vt)}\cdot(T/Tnom)^{XTI/NC}$$

$$\mathbf{ISS}(T) = (\mathbf{ISS}/(T/Tnom)^{XTB})\cdot e^{(T/Tnom-1)\cdot EG/(NS\cdot Vt)}\cdot(T/Tnom)^{XTI/NS}$$

$$\mathbf{BF}(T) = \mathbf{BF}\cdot(T/Tnom)^{XTB}$$

$$\mathbf{BR}(T) = \mathbf{BR}\cdot(T/Tnom)^{XTB}$$

$$\mathbf{RE}(T) = \mathbf{RE}\cdot(1+\mathbf{TRE1}\cdot(T-Tnom)+\mathbf{TRE2}\cdot(T-Tnom)^2)$$

$$\mathbf{RB}(T) = \mathbf{RB}\cdot(1+\mathbf{TRB1}\cdot(T-Tnom)+\mathbf{TRB2}\cdot(T-Tnom)^2)$$

$$\mathbf{RBM}(T) = \mathbf{RBM}\cdot(1+\mathbf{TRM1}\cdot(T-Tnom)+\mathbf{TRM2}\cdot(T-Tnom)^2)$$

$$\mathbf{RC}(T) = \mathbf{RC}\cdot(1+\mathbf{TRC1}\cdot(T-Tnom)+\mathbf{TRC2}\cdot(T-Tnom)^2)$$

$$\mathbf{VJE}(T) = \mathbf{VJE}\cdot T/Tnom - 3\cdot Vt\cdot\ln(T/Tnom) - Eg(Tnom)\cdot T/Tnom + Eg(T)$$

$$\mathbf{VJC}(T) = \mathbf{VJC}\cdot T/Tnom - 3\cdot Vt\cdot\ln(T/Tnom) - Eg(Tnom)\cdot T/Tnom + Eg(T)$$

$$\mathbf{VJS}(T) = \mathbf{VJS}\cdot T/Tnom - 3\cdot Vt\cdot\ln(T/Tnom) - Eg(Tnom)\cdot T/Tnom + Eg(T)$$

where $Eg(T)$ = silicon bandgap energy = $1.16 - .000702\cdot T^2/(T+1108)$

$$\mathbf{CJE}(T) = \mathbf{CJE}\cdot(1+\mathbf{MJE}\cdot(.0004\cdot(T-Tnom)+(1-\mathbf{VJE}(T)/VJE)))$$

$$\mathbf{CJC}(T) = \mathbf{CJC}\cdot(1+\mathbf{MJC}\cdot(.0004\cdot(T-Tnom)+(1-\mathbf{VJC}(T)/VJC)))$$

$$\mathbf{CJS}(T) = \mathbf{CJS}\cdot(1+\mathbf{MJS}\cdot(.0004\cdot(T-Tnom)+(1-\mathbf{VJS}(T)/VJS)))$$

The collector, base, and emitter parasitic resistances have no temperature dependence.

Noise

Noise is calculated assuming a one hertz bandwidth, using the following spectral power densities (per unit bandwidth):

the parasitic resistances generate thermal noise ...

$Ic^2 = 4 \cdot k \cdot T/(RC/area)$

$Ib^2 = 4 \cdot k \cdot T/Rb$

$Ie^2 = 4 \cdot k \cdot T/(RE/area)$

the base and collector currents generate shot and flicker noise ...

$Ib^2 = 2 \cdot q \cdot Ib + KF \cdot Ib^{AF}/FREQUENCY$

$Ic^2 = 2 \cdot q \cdot Ic + KF \cdot Ic^{AF}/FREQUENCY$

References

For a more complete description of bipolar transistor models, refer to

[1] Ian Getreu, *Modeling the Bipolar Transistor*, Tektronix, Inc. part# 062-2841-00.

Resistor

General Form R<*name*> <(+) *node*> <(-) *node*> [*model name*] <*value*>

Examples

RLOAD 15 0 2K

R2 1 2 2.4E4

Model Form .MODEL < *model name*> RES [*model parameters*]

(+) and (-) nodes

Define the polarity when the resistor has a positive voltage across it. Positive current flows from the (+) node through the resistor to the (-) node.

[*model name*] If this is included and **TCE** (in the model) **is not specified**, then the resistance is given by the formula

$$<value>\cdot R\cdot(1+\mathbf{TC1}\cdot(T-Tnom)+\mathbf{TC2}\cdot(T-Tnom)^2)$$

where <*value*> is normally positive (though it can be negative, but **not** zero). If [*model name*] is included and **TCE** (in the model) **is specified**, then the resistance is given by the formula

$$<value>\cdot R\cdot 1.01^{TCE\cdot(T-Tnom)}$$

where <*value*> is normally positive (though it can be negative, but **not** zero). “Tnom” is the nominal temperature (set using TNOM option).

Table 2-20 *Resistor Model Parameters*

Model Parameters	Description	Units	Default
R	Resistance multiplier		1
TC1	Linear temperature coefficient	°C -1	0
TC2	Quadratic temperature coefficient	°C -2	0
TCE	Exponential temperature coefficient	%/°C	0

Noise

Noise is calculated assuming a one hertz bandwidth. The resistor generates thermal noise using the following spectral power density (per unit bandwidth)

$$i^2 = 4\cdot k\cdot T/\text{resistance}$$

Voltage-Controlled Switch

General Form

S<*name*> <(+) *switch node*> <(-) *switch node*>
\+ <(+) *controlling node*> <(-) *controlling node*>
\+ <*model name*>

Examples

```
S12     13   17    2   0    SMOD
SESET   5     0  15   3    RELAY
```

Model Form

.MODEL < *model name*> VSWITCH [*model parameters*]

The voltage-controlled switch is a special kind of voltage-controlled resistor. The resistance between the <(+) *switch node*> and <(-) *switch node*> depends on the voltage between the <(+) *controlling node*> and <(–) *controlling node*>. The resistance varies continuously between the **RON** and **ROFF** model parameters.

A resistance of 1/GMIN is connected between the controlling nodes to keep them from floating. See the .OPTIONS statement (page 1-26) for setting GMIN.

We have chosen this model for a switch to try to minimize numerical problems. However, there are a few things to keep in mind:

With double precision numbers *Pspice* can handle only a dynamic range of about 12 decades. So, we do not recommend making the ratio of **ROFF** to **RON** greater than 1E+12.

Similary, we do not recommend making the transition region too narrow. Remember that in the transition region the switch has gain. The narrower the region, the higher the gain and the greater the potential for numerical problems.

Although very little computer time is required to evaluate switches, during transient analysis the simulator must step through the transition region using a fine enough step size to get an accurate waveform. Applying many transitions can produce long run times when evaluating the other devices in the circuit at each time step.

RON and **ROFF** must be greater than zero and less than 1/GMIN.

Table 2-21 *Voltage-Controlled Switch Model Parameters*

Model Parameters	Description	Units	Default
ROFF	"Off" resistance	ohm	1E+6
RON	"On" resistance	ohm	1.0
VOFF	Control voltage for "off" state	volt	0.0
VON	Control voltage for "on" state	volt	1.0

Equations

In the following equations:

Vc = voltage across control nodes
Lm = log-mean of resistor values = $ln((\mathbf{RON}\cdot\mathbf{ROFF})^{1/2})$
Lr = log-ratio of resistor values = $ln(\mathbf{RON}/\mathbf{ROFF})$
Vm = mean of control voltages = $(\mathbf{VON}+\mathbf{VOFF})/2$
Vd = difference of control voltages = **VON**-**VOFF**
k = Boltzmann's constant
T = analysis temperature (°K)

Switch Resistance

Rs = switch resistance

If: **VON** > **VOFF**

For: Vc ≥ **VON**
Rs = **RON**
For: Vc ≤ **VOFF**
Rs = **ROFF**
For: **VOFF** < Vc < **VON**
$Rs = exp(Lm + 3\cdot Lr\cdot(Vc-Vm)/(2\cdot Vd) - 2\cdot Lr\cdot(Vc-Vm)^3/Vd^3)$

If: **VON** < **VOFF**

For: Vc ≤ **VON**
Rs = **RON**
For: Vc ≥ **VOFF**
Rs = **ROFF**
For: **VOFF** > Vc > **VON**
$Rs = exp(Lm - 3\cdot Lr\cdot(Vc-Vm)/(2\cdot Vd) + 2\cdot Lr\cdot(Vc-Vm)^3/Vd^3)$

Noise

Noise is calculated assuming a one hertz bandwidth. The voltage-controlled switch generates thermal noise as if it were a resistor having the same resistance that the switch has at the bias point, using the following spectral power density (per unit bandwidth)

$$i^2 = 4\cdot k\cdot T/Rs$$

Transmission Line

General Form

T<*name*> <A *port* (+) *node*> <A *port* (-) *node*>
+ <B *port* (+) *node*> <B *port* (-) *node*>
+ Z0=<*value*> [TD=<*value*>] [F=<*value*> [NL=<*value*>]]

Examples

T1 1 2 3 4 Z0=220 TD=115ns
T2 1 2 3 4 Z0=220 F=2.25MEG
T3 1 2 3 4 Z0=220 F=4.5MEG NL=0.5

Model Form

.MODEL < *model name*> TRN [*model parameters*]

Figure 2-9 *Transmission Line Model*

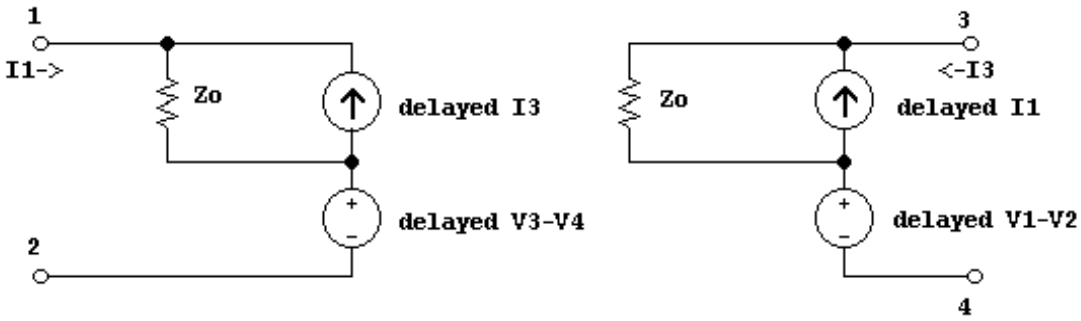


Table 2-22 *Transmission Line Model Parameters*

Model Parameters	Description	Units	Default
ZO	Characteristic impedance	ohms	none
TD	Transmission delay	seconds	none
F	Frequency for NL	Hz	none
NL	Relative wavelength	none	.25

As shown in Figure 2-22, the transmission line device is a bidirectional, delay line. It has two ports, A and B. The (+) and (-) nodes define the polarity of a positive voltage at a port. In Figure 2-12, port A's (+) and (-) nodes are one and two, and port B's (+) and (-) nodes are three and four, respectively.

Z0 is the characteristic impedance. The transmission line's length can be specified either by TD, a delay in seconds, or by F and NL, a frequency and a relative wavelength at F. NL defaults to 0.25 (F is then the quarter-wave frequency). Although TD and F are both shown as optional, one of the two must be specified. Examples T1, T2, and T3 all specify the same transmission line.

Note Both Z0 ("zee-zero") and ZO ("zee-oh") are accepted by the simulator.

During transient (.TRAN) analysis, the internal time step is limited to be no more than one-half the smallest transmission delay, so short transmission lines cause long run times.

Digital Device

General Form

U<*name*> <*type*> ([*parameter value*]) <*node*>
\+ [*timing model name*] <IO *model name*>

U<*name*> STIM *(<width value>,<format value>) <node>*
+ *<*IO *model name> [*TIMESTEP*=<stepsize value>]*
+ *<waveform description>*

Examples

```
U1   NAND(2)   1   2    10   DO_GATE   IO_DFT
U2   JKFF(1)   3   5   200   3   3   10   2   D_293ASTD   IO_STD
U3   STIM(1,1)   110   STMIOMDL   TIMESTEP=10NS
+          0nS,   1
+         40nS,   0
```

Table 2-23 *Digital Device Model Parameters*

Model Parameters	Description	Units	Default
INLD	Input load capacitance	farad	0
OUTLD	Output load capacitance	farad	0
DRVH	Output high level resistance	ohm	0
DRVL	Output low level resistance	ohm	0
AtoD	Name of AtoD subcircuit		none
DtoA	Name of DtoA subcircuit		none

Note

The digital devices are part of the *Digital Simulation* option for *Pspice.* For more information on these devices see the “Digital Simulation” chapter.

Current-Controlled Switch

General Form

W<*name*> <(+) *switch node*> <(-) *switch node*>
\+ <*controlling V device name*> <*model name*>

Examples

```
W12      13   17   VC   WMOD
WRESET    5    0   VRESET   RELAY
```

Model Form

.MODEL < *model name*> ISWITCH [*model parameters*]

Table 2-24 *Current-Controlled Switch Model Parameters*

Model Parameters	Description	Units	Default
IOFF	Control current for “off” state	amp	0.0
ION	Control current for “on” state	amp	1E-3
ROFF	“Off” resistance	ohm	1E+6
RON	“On” resistance	ohm	1.0

The current-controlled switch is a special kind of current-controlled resistor.

<*controlling V device name*>

The resistance between the <(+) *switch* node and <(-) *switch* node> depends on the current through <*controlling V device name*>.

The resistance varies continuously between **RON** and **ROFF**.

RON and **ROFF**

Must be greater than zero and less than 1/GMIN.

A resistance of 1/GMIN is connected between the controlling nodes to keep them from floating. See the .OPTIONS statement (page 1-26) for setting GMIN.

This model was chosen for a switch to try to minimize numerical problems. However, there are a few things that must be evaluated:

Using double precision numbers, the simulator can handle only a dynamic range of about 12 decades. Therefore, it is not recommended making the ratio of **ROFF** to **RON** greater than 1E+12.

Similarly, it is also not recommended making the transition region too narrow. Remembering that in the transition region the switch has gain. The narrower the region, the higher the gain and the greater the potential for numerical problems.

Although very little computer time is required to evaluate switches, during transient analysis the simulator must step through the transition region using a fine enough step size to get an accurate waveform. Having many transitions can produce long run times when evaluating the other devices in the circuit for many times.

In the following equations:

Ic	= controlling current
Lm	= log-mean of resistor values = $ln((\mathbf{RON}\cdot\mathbf{ROFF})^{1/2})$
Lr	= log-ratio of resistor values = $ln(\mathbf{RON}/\mathbf{ROFF})$
Im	= mean of control currents = (**ION**+**IOFF**)/2
Id	= difference of control currents = **ION**-**IOFF**
k	= Boltzmann's constant
T	= analysis temperature (°K)

Switch Resistance

Rs = switch resistance

If: **ION** > **IOFF**

For: Ic ≥ **ION**

Rs = **RON**

For: Ic ≤ **IOFF**

Rs = **ROFF**

For: **IOFF** < Ic < **ION**

$$Rs = exp(Lm + 3 \cdot Lr \cdot (Ic-Im)/(2 \cdot Id) - 2 \cdot Lr \cdot (Ic-Im)^3 / Id^3)$$

If: **ION** < **IOFF**

For: Ic ≤ **ION**

Rs = **RON**

For: Ic ≥ **IOFF**

Rs = **ROFF**

For: **IOFF** > Ic > **ION**

$$Rs = exp(Lm - 3 \cdot Lr \cdot (Ic-Im)/(2 \cdot Id) + 2 \cdot Lr \cdot (Ic-Im)^3 / Id^3)$$

Noise

Noise is calculated assuming a one hertz bandwidth. The current-controlled switch generates thermal noise as if it were a resistor using the same resistance as the switch has at the bias point, using the following spectral power density (per unit bandwidth)

$$i^2 = 4 \cdot k \cdot T/Rs$$

Subcircuit Instantiation

General Form X<*name*> [node]* <*subcircuit name*>

Examples
```
X12    100  101  200  201  DIFFAMP
XBUFF  13   15   UNITAMP
```

<*subcircuit name*>

The <*subcircuit name*> is the name of the subcircuit's definition (see .SUBCKT statement).
There must be the same number of nodes in the call as in the subcircuit's definition. This statement causes the referenced subcircuit to be inserted into the circuit using the given nodes to replace the argument nodes in the definition. It allows a block of circuitry to be defined once and then used in several places.

Subcircuit references can be nested. That is, a call can be given to subcircuit A, whose definition contains a call to subcircuit B. The nesting can be to any level, but must not be circular: for example, if subcircuit A's definition contains a call to subcircuit B, then subcircuit B's definition must not contain a call to subcircuit A.